Digital storage oscilloscope
PM3310

Service manual

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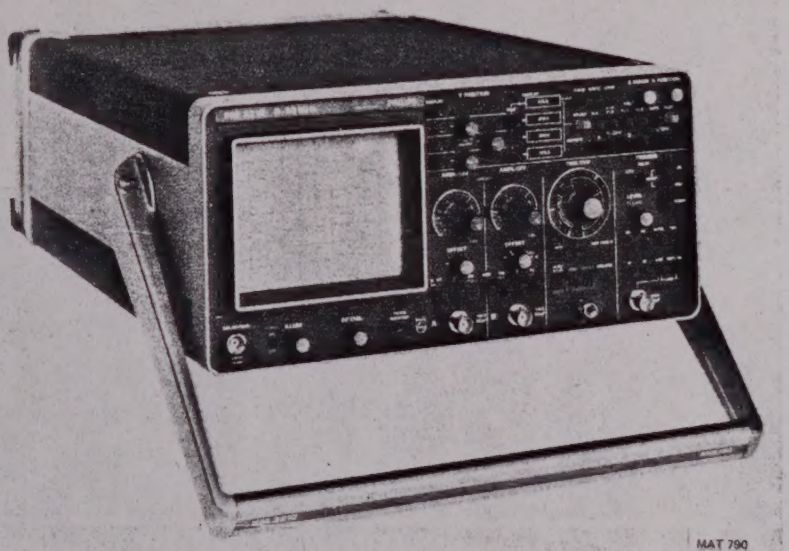

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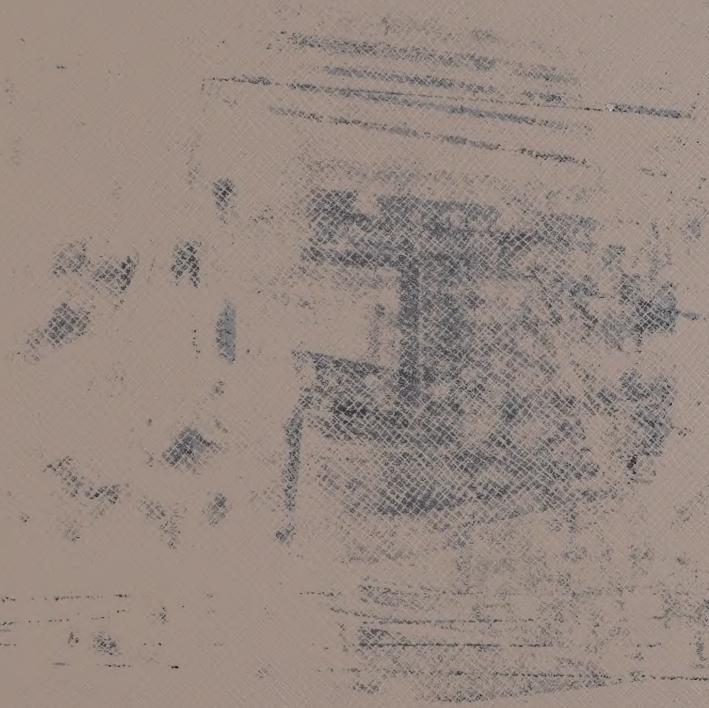

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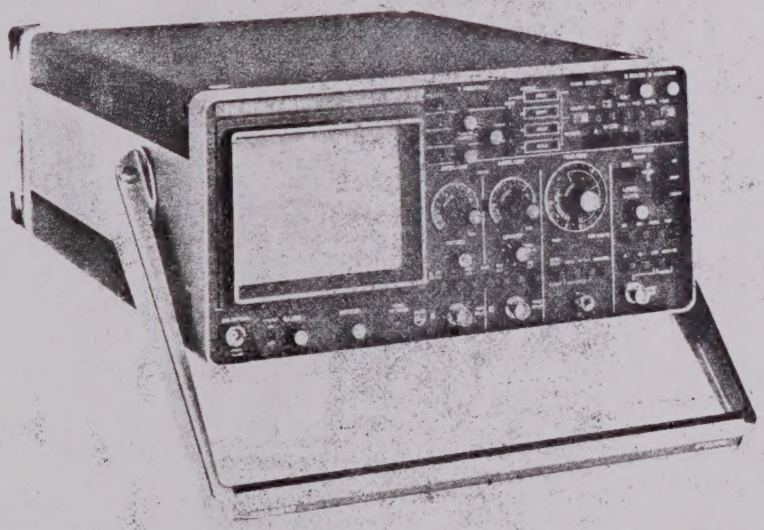

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6. CIRCUIT DESCRIPTIONS

6.1. BLOCK DIAGRAM DESCRIPTION

This chapter serves to explain the main functions of the oscilloscope. The working principle is divided into four sections:

6.1.1. Acquisition system
6.1.2. Display system
6.1.3. Microprocessor and software
6.1.4. Power supply

6.1.1. Acquisition system

By means of the acquisition system the analog input signals are converted into digital information.
Before conversion the analog signals must be adapted so that an Analog to Digital Converter (ADC) is able to convert them. This system can be divided into the following sections:

6.1.1.1. The vertical channels
6.1.1.2. The analog-to-digital convertor (including P^2CCD)
6.1.1.3. Trigger and trigger delay circuits
6.1.1.4. The sampling system
6.1.1.5. The time base system
6.1.1.6. The acquisition control

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IMPORTANT

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

NOTE: *The design of this instrument is subject to continuous development and improvement. Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.*

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4.2. CHARACTERISTICS

This instrument has been designed and tested in accordance with IEC Publication 348 for Class 1 instruments and has been supplied in a safe condition. The present Instruction Manual contains information and warnings that shall be followed by the purchaser to ensure safe operation and to retain the instrument in a safe condition.

- This specification is valid after the instrument has warmed up for 30 minutes (reference temperature 23 °C).
- Properties expressed in numerical values with tolerance stated, are guaranteed by the manufacturer. Numerical values without tolerances are typical and represent the characteristics of an average instrument.
- Inaccuracies (absolute or in %) relate to the indicated reference value.

Designation	*Specification*	*Additional information*
C.R.T.		
Cathode ray tube	D14 - 292 GH/39	
Accelerating voltage	10 kV	
Screen size	8 x 10 cm	Metal backed
Phosphor type	P31 (GH)	
Graticule	Internal	With centimeter divisions and 2 mm subdivisions along the central vertical axis shorter 2 mm divisions along the second, fourth, sixth and eight horizontal axis.
Graticule illumination	Clearly visible under normal light conditions and continuously variable	
Trace rotation	Front panel screwdriver adjustment	
Focus	Adjusted automatically	
Input vertical		
Frequency range	d.c. 0 ... 60 MHz a.c. 10 Hz ... 60 MHz	
Rise-time	< 6 ns	
Pulse aberrations	± 3 %	Measured in Y-expand with a test pulse of 8 div; rise-time 1 ns; frequency 1 MHz (except first 0.2 cm measured from mid pulse)
Vertical deflection		
Defl. coeff.	10 mV/div ... 50 V/div	12 Calibrated positions in 1-2-5 sequence
Error limit	± 3 %	±5 % in Y - expand
Continuous control range	1 : > 2.5	
Input impedance	1 MΩ // 25 pF	
Coupling	a.c. - 0 - d.c.	
Max. perm. input voltage	± 400 V	d.c. + a.c. peak
Input selection	A only B only Add A and B	Channel B can be inverted

C.M.R.R.	100 : 1	At 2 MHz max. common mode signal 8 div.
Dynamic range	2x voltage range	
DC offset	± 4x voltage range	
Max. sample rate	50 MHz	
Visible signal delay	> 10 ns	See also "delay"
Time-base		
Time coefficients		
Repetitive only	5 ns ... 0.2 µs/div	
Direct	0.5 µs ... 0.2 s/div	
Roll	0.5 s ... 60 min/div	
Coefficient error	< 2 %	4% combined with delay in "REPETITIVE ONLY"
Resolution	25 samples/div	
Triggering		
Source	A B EXT EXT : 10 Line	
Sensitivity		
Internal	0.3 div 0.15 div	at 60 MHz at 40 MHz
External	0.3 V 0.15 V	at 60 MHz at 40 MHz
Ext : 10	3 V 1.5 V	at 60 MHz at 40 MHz
Slope	+/–	
Modes	Auto d.c. a.c. TV-frame (1/1 picture)	20 Hz ... 60 MHz dc ... 60 MHz 10 Hz ... 60 MHz Acc. to CCIR (625 lines)
Level		
Auto	Proportional to peak-to-peak value of trigger signal	
a.c./d.c.	± 3 div	
Delay		
Range	–9 ... +9999 div 0 ... 100 div	0.2 s ... 0.5 µs/div 0.2 µs ... 5 ns/div
Accuracy	±2 mm or 0.01 % ±2 div + visible delay	0.2 s ... 0.5 µs/div 0.2 µs ... 5 ns/div
Input impedance	1 MΩ // 25 pF	
Max. input voltage	± 400 V	dc + ac peak

Memory

Number of memories	4	1 accumulator memory and 3 store memories
Resolution horizontal	1 : 250	In single trace mode
Resolution vertical	1 : 250	

Operation modes

Single	Refreshment of accumulator mem. takes place, when trigger level is reached and time set with trigger delay has been passed. Signal is stored according to position of trigger delay. During waiting time accumulator, is displayed and LED "NOT TRIG'D" lights up.	0.5 µs ... 0.2 s/div
Recurrent	Signal in accumulator memory is displayed on the screen. After the time set with the trigger delay the memory is over-written by new information.	5 ns . . . 0.2 s/div
Roll	Signal is built-up point by point at the right-hand side of the screen and moves to the left. When accumulator is completely filled, information is placed in register 3, next in 2, then in 1 and next in accumulator. After this, roll-mode stops, indicated by flashing "RUN" light.	0.5 s ... 60 min/div
Multiple	4 times single with "SAVE" in memories	0.5 µs ... 0.2 s/div

Display modes

Memory	Covers 2 div. screen height	
Channel display combinations		
Accumulator	Depends on input selection	
Register	Information as stored in accumulator can be selected for storage in each of the three register memories and is displayed if display button is depressed.	Total information held in STORE 1, 2 or 3 can be inverted.
Vertical position range	± 8 div	
Vertical expand	5 x	Memory covers 10 cm screen height. Indicated via LED in display section.
Horizontal expand	1 : > 2.5	Continuous
X-Y selection	Deflection in X-direction can be derived from time base or from memory contents derived from A-input	

Memory modes	Clear	Accumulator memory is cleared
	Save (3x)	Contents of accumulator memory are stored in selected register
	Write	Input signal can be written in accumulator memory
	Lock	Memory system is closed
Dot join	Pushbutton	Changes normal display mode (dot-join) into display of only dots.

Plot output

Horizontal	1 V / full scale	
Vertical	1 V / full scale	
Pen lift	TTL comp. "0" = unblanked (pen down) "1" = blanked (pen up)	open collector output max. load 0,5V at 500 mA cont.
Plot time	approx. 100 s.	
Plot sequence	B plot after A plot	

Interfaces

IEC-Bus	Optional by means of a plug-in p.c. board	
IEC-Bus	Settings and output controllable from bus-line controller	
Local/Remote	With IEC connector.	

X-Y Display

Y f(t)	From time-base	
Y f(x)	From YA input	Dot join is not in operation
Bandwidth	See YA	
Accuracy	< 5 %	Tube included
Phase difference	Distance between signal derived from A and signal derived from B is 1/25 div.	
Position	0 of stored A signal will be at centre of screen	

Calibration output

Frequency	2.5 kHz
Voltage	3 V
Current	6 mA

Power supply

Line voltage	100 ... 120 V ± 10 % 220 ... 240 V ± 10 %
Line frequency	50 ... 400 Hz ± 10 %
Power consumption	< 65 W

Battery		
Function	For memory back-up only	
Type	2 pen light batteries of 1.5 V	For instance 2 x 1.5 V Lithium SAFT 2 x 1.5 V Duracell
Insulation	The insulation of the power supply fulfils the safety requirements of IEC 348 cl. I for metal-encased instruments	

Environmental characteristics

Note: The characteristics are valid only if the instrument is checked in accordance with the official checking procedure. Details on these procedures and failure criteria are supplied on request by the PHILIPS-organisation in your country, or by N.V. PHILIPS' GLOEILAMPENFABRIEKEN, TEST AND MEASURING DEPARTMENT, EINDHOVEN, THE NETHERLANDS.

Ambient temperature	+ 5 °C ... +40 °C −10 °C ... +40 °C −55 °C ... +75 °C	Rated range of use Operating temperature range Storage temperature in accordance with MIL 28800 and a maximum at 24 hours on high and low temperature
Altitude		
Operating	5000 m (15000 ft)	In accordance with IEC 68-2-13 test M
Non-operating	15000 m (50000 ft)	
Humidity	Acc. IEC 68 Db	Instrument withstands 95 % RH over a temperature cycle of 25 °C to 40 °C (non-operating)
Shock	30 m/s^2	Operating; half sine-wave shock of 11 ms duration; 3 shocks per direction for a total of 18 shocks.
Vibration	3 m/s^2	Operating; vibrations in three directions with a maximum of 20 min. per direction; 10 minutes with a frequency of 5 - 25 Hz and amplitude of 1.016 mm p-p; 10 min with a frequency of 25 - 55 Hz and an amplitude of 0.5 mm p-p. An extra 10 minutes of the resonant of frequency with the highest rise in amplitude. Unit mounted on vibration table without shock absorbing material.
Dimensions	Length 460 mm Width 316 mm Height 154 mm	Handle and controls excluded Handle excluded Feet excluded See also Fig. 1.2.
Weight	Approx. 12 kg	

4. GENERAL INFORMATION

4.1. INTRODUCTION

The PM 3310 Digital Storage Oscilloscope is a portable, two-channel 60 MHz measuring instrument featuring micro-processor controlled electronic circuits.

A compact ergonomic design facilitates the extensive measuring capabilities of the instrument.
The versatile circuit arrangement combined with the software of the micro-processor gives a wide range of facilities, including:

- Brilliant display.
- Pre-trigger view.
- Storage of two channels with four different "event" signals per channel.
- IEC-bus optional (with the aid of PM 3325).
- Plotter output.
- Trigger delay.
- Memory back-up (batteries not included).

Furthermore, a large 8 cm x 10 cm screen with illuminated graticule lines provides for easier viewing, a 10 kV accelerating potential giving a high-intensity trace with a well-defined spot.
The oscilloscope is provided with numerous integrated circuits, which ensure stable operation and reduce the number of adjusting points.

The supply voltage can be set to one of two ranges: 100 ... 120 V ± 10 % or 220 ... 240 V ± 10 %.
As a result of the features listed above, the oscilloscope is suitable for a wide range of applications, for example the measurement and observation of:

- Rise-time (gives brilliant display intensity).
- Fast signals with a very low repetition rate.
- Very low frequency signals (up to 1 hour per division).

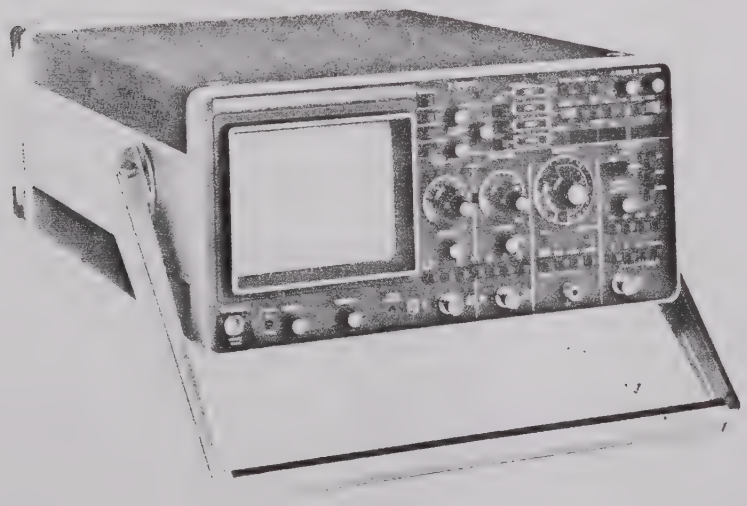

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Fig. 1.1. 60 MHz Digital storage oscilloscope PM 3310

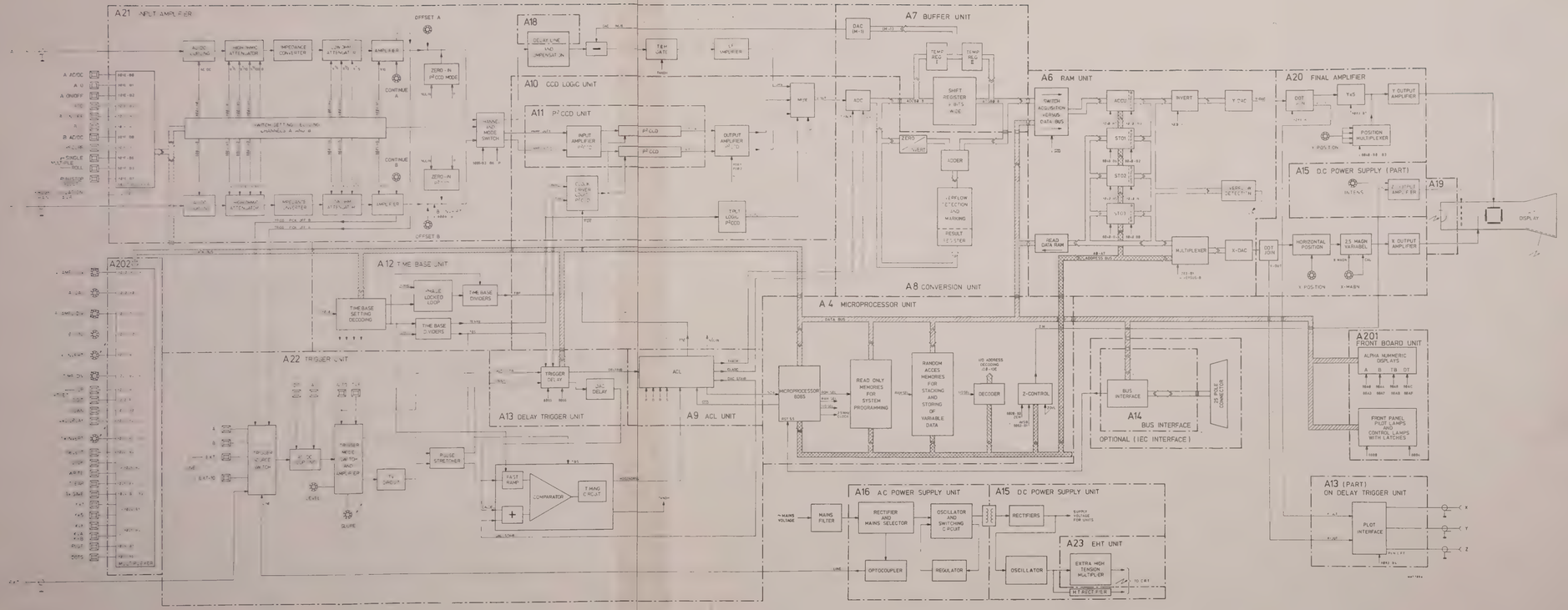


Fig. 6.1.1.

6.1.1.1. The vertical channels (unit A21 page 6–188)

The vertical channel consist of two identical channels A and B except for the possibility B invert.
The sensitivity range is 10 mV/div ... 50 V/div in a 1-2-5 sequence.
All front panel settings of the vertical channels except for the CONTINUE an OFFSET controls are read each main loop of the program of the microprocessor system via multiplexers.
After calculation in the microprocessor, the settings are written into the switch setting decoding. This decoding generates the signals to set the ac/dc coupling, the high and low ohmic attenuators and the amplifier gain according to the front panel settings. Moreover these settings can be determined by the IEC Bus interface option.
The input signal is applied to the channel switch via the ac/dc coupling, the high ohmic attenuator, the impedance convertor, the low ohmic attenuator and the amplifier.
Just after the amplifier a zero in signal NULLIN for P^2CCD mode operation is applied to the channel switch.
For time base settings of 3600 s/div. 0.5ms/div . and 0.2 µs/div . 5 ns/div the channel switch connects the signal to the delay line.
In dual channel mode (A and B) the microprocessor system generates via the switch setting decoding the signals A ON and B ON in such a way, that a chopped signal is applied to the delay line. The output of the delay line is connected to a compensation network to correct the faults introduced by the delay line.

6.1.1.2. The analog-to-digital convertor (including P^2CCD) (unit A10 + A11 page 6–110 and page 6–122).

The output signal of the delay line is applied to the T&H (Track and Hold) gate via a subtractor.
This T&H gate tracks the input signal continuously and at a command TANDH its output is held to the momentary value of the input signal for about 4 µseconds. The signal TANDH is generated on the trigger unit and will be described later. Via a low frequency amplifier and a multiplexer the output signal of the T&H gate is applied to the sample and hold gate of an ADC in which the output signal of the T&H gate is taken over and held to the same value for at least the conversion time.
The ADC is controlled by the signals TRACK and CLADC which are generated at the Acquisition Control Logic A9 (ACL).

To eliminate faults of the ADC conversion a correction takes place.
In ROLL, DIRECT and SAMPLING (see operating manual and chapter 6.1.1.6.) mode the correction functions as follows:

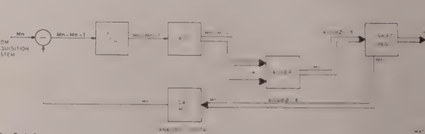


Fig. 6.1.2.

To reduce errors in conversion, analog samples for digitising are compared with preceding samples, these being subtracted so that only small increments are converted to digital values in the ADC. After conversion, the digital equivalent of the original analog signal is produced by adding the differential signal from the ADC to the digital value of the preceding sample.
Referring to the block diagram, M_n is the new sample of the input signal from the acquisition system; M_{n-1} is the preceding sample, derived from the shift register and re-converted by DAC M-1 to analog form. At the input to the Track and Hold circuit, M_{n-1} is subtracted from M_n to produce a differential analog voltage, which is then converted to digital form in the ADC and added to the preceding digital value M_{n-1}.

$$\text{i.e. } (M_n - M_{n-1}) + M_{n-1} = M_n$$

After this procedure, the adder output value M_n will be shifted into a shift register as a new and corrected value. This system of digital adding is also used, in a different way, in the P²CCD-mode as described below.

For time base settings of 0.2 ms/div - 0.5 µs/div the instrument operates in P²CCD mode. P²CCD means Profiled Peristaltic Charge Coupled Device in which an input signal can be written-in at a high speed and afterwards can be read out at a low speed.

If the instrument operates in P²CCD mode, the output of the channel selector is applied to the input amplifier of the P²CCD. Because of the principle of the P²CCD in dual channel mode the signals – A and + B are applied as P AMP OUT 1 and P AMP OUT 2 resp. The P²CCD contents is read out by a 78 kHz signal and written in by a Time Base Fast (TBF) pulse via the clock driver input logic. The output of the P²CCD is amplified and applied to a multiplexer which switches between the two P²CCD outputs. So in the P²CCD mode the chopper switch of the channel switch is inoperative.
Output VOUT of the multiplexer is applied to the sample and hold gate of the ADC.

Due to internal P²CCD faults and differences between the frequencies f_{in} and f_{out}, an incorrect zero level of the P²CCD output signal is possible as shown in the following graph.

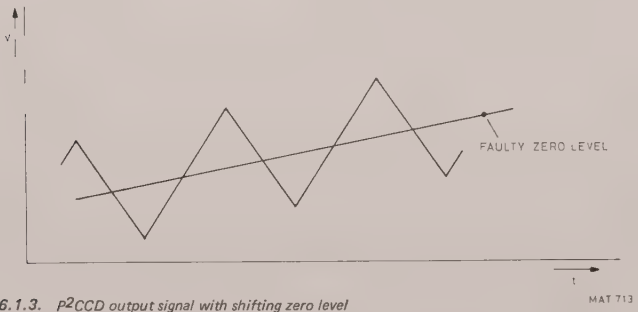


Fig. 6.1.3. P²CCD output signal with shifting zero level

Under these conditions, the total faulty contents of the P²CCD are converted from analog form to digital in 256 steps and after each conversion the data is put on the ADCBØ ... ADCB8 bus and directly shifted into the 9-bit shift register on buffer unit A7. After 256 steps, the total P²CCD contents are stored here, and the register is then blocked.

In order to correct the zero level, the P²CCD input is switched to zero by a signal NULIN and 256 samples of this zero signal are shifted into the P²CCD at the same frequency f_{in} as for the normal input signal.

By reading the P2CCD contents again, with the same frequency f_{out} (78 kHz) as for the faulty ADC input signal, an incorrect zero level having the same errors as described above will appear on the P2CCD output as shown below.

Fig. 6.1.4.

This incorrect zero level is then digitally subtracted (in 256 steps) from the faulty ADC input signal, which was already stored in the shift register.
The corrected result is then re-stored in the shift register.

6.1.1.3. Trigger and trigger delay circuits (unit A22 page 6–211)

In the trigger channel a signal derived from one of the sources A, B, external or line is applied to the AC/DC switch. The output of this switch is applied to the automatic level circuit which determines the peak-peak value. If automatic triggering is selected the peak-peak value is applied to the level potentiometer to obtain the possibility to level over the complete signal.
In the modes AC or DC a constant voltage is applied to the level potentiometer. In TVF mode the same voltage is applied to both sides of the potentiometer so that leveling is inoperative.
The slope determines which voltage is selected; positive or negative peak voltage.
After amplification the slope is selected and the trigger signal is applied to the pulse stretcher. The TV path in parallel applies its output signal also to the pulse stretcher.
If the TV signal contains equalisation pulses there is a selection to odd or even frame pulses. Otherwise only frame pulses are available at the output.
The pulse stretcher output signal is applied to two circuits: the sampling circuit and the trigger delay circuit.
The trigger delay circuit contains a down counter of which the loading is effected by the microprocessor system via an output port with a value derived from the front panel settings in combination with the TIME/DIV switch setting. Upon the receipt of a trigger pulse from the trigger circuit the down-counter starts counting time base pulses (see also 6.1.1.5.) until its zero state is reached. This effects in a pulse which blocks the reading of new information in the shift register. After this the shift register contents can be copied in the ACCU memory.

6.1.1.4. The sampling system (unit A22 page 6–211)

In sampling mode the output of the pulse stretcher is controlling the fast ramp generator. The ramp is determined by the TIME/DIV switch setting via the microprocessor and the control signals LØ ... L2. The fast ramp output is applied to a comparator. At the other input of the comparator a signal DACSTAIR is applied which is a stair case voltage derived from the ACL counter that increases one step every time that a conversion is completed and a COUNT pulse is counted by the ACL counter. To this staircase voltage a voltage called DACDEL is added which is derived from the trigger delay unit. This is a voltage proportional to the preset trigger delay.
If now the fast ramp voltage reaches the same potential as the sum of DACDEL and DACSTAIR, the system generates a HOCON (Hold and convert) and a TANDH (Track and hold) pulse to start an analog to digital conversion. If a conversion is completed the output of the pulse stretcher is enabled to generate via the fast ramp generator a new HOCONDRS pulse to start the next conversion. Now the DACSTAIR signal will be increased one stair level so this conversion takes place at the following point of the repetitive input signal.

6.1.1.5. The time base system (unit A12 page 6–135)

With respect to an ordinary oscilloscope this digital storage oscilloscope does not need a sawtooth time base generator because the position on the screen is determined digitally.
Therefore the time-base system consists mainly of frequency dividers.
The base frequency is 2.5 MHz derived from the cristal clock frequency of the microprocessor system.
Because the need of higher frequencies then 2.5 MHz a voltage controlled oscillator is introduced with a frequency of 100 MHz. This frequency is kept stable by dividing it by a factor of 80 and to compare it with the microprocessor clockpulse divided by a factor of 2. Now both signals have a frequency of 1.25 MHz and via a feedback loop the VCO is controlled.
For the P2CCD mode a TBF signal is generated and in DIRECT and ROLL mode a TBS signal.
The dividing factors, so the frequencies of the TBF and TBS signals, are determined by the setting of the TIME/DIV switch which is decoded by the time base setting decoding.
The frequency of the TBF and TBS signals is such that for one horizontally division on the screen exactly 25 TBF or TBS periods are generated.

6.1.1.6. The acquisition control (unit A9 page 6–92)

The most important part of the acquisition control is a counter which counts the number of conversions by counting COUNT pulses.
Each conversion is initiated by a HOCON (hold and convert pulse) and results after completion into a COUNT pulse.
So it is counting how many input values are written into the shift register.

The acquisition control is operating in a different way for each of the four system modes DIRECT (D) - ROLL (R) - SAMPLING (S) and P2CCD (P).
In each of these four modes NDR (New Data Ready) pulses are generated to indicate to the microprocessor that new data is ready and can be copied in the ACCU memory.
The microprocessor in turn answers with SOD pulses telling that the copying of new information into the ACCU memory is completed and that new information can be stored in the shift register.

Direct mode

After a hold-off period in which at least 256 new input signal samples are shifted into the shift register, so after a total refreshment of the shift register contents the acquisition system is enabled to react on a new trigger pulse.
Upon the receipt of such a trigger pulse a NDR pulse will be generated just after the completion of the last conversion.

ROLL-mode

The ROLL-mode action is started when ROLL-mode is selected and the front panel R/S pushbutton is depressed. This results in the generation of TBS pulses by the time-base unit. These TBS pulses are converted by the trigger unit in HOCONDRS (Hold and convert) pulses which are used in the ACL unit to initiate the conversions of new input signal samples.
After each completed conversion a COUNT pulse is generated and so a NDR pulse.

On each NDR pulse the total shift register contents are copied into the RAM memory and in the same time the shift register output information is shifted again into this shift register by coupling the output of the shift register directly to its input.
Furthermore ROLL-mode functions are under the control of the software.
The software counts the number of NDR pulses and after 256 NDR pulses it saves the ACCU contents into STO3, after again 256 pulses into STO2, then into STO1. After in total 4 x 256 pulses the software stops the ROLL-mode action and indicates this by generating a flashing command for the RUN lamp.

Sampling mode

In sampling mode a HOCONDRS pulse is generated on each incoming TRIST pulse except for those coming within the hold-off period. These HOCONDRS pulses initiate conversions of the input signal samples.
After 256 samples are converted and stored in the shift register a NDR pulse is generated and the shift register contents are copied into the ACCU memory.
The microprocessor generates a $\overline{\text{SOD}}$ signal after this copying, the ACL counter is reset to zero and the system reacts again on new incoming triggers.

P2CCD-mode

After reading in at least 256 samples of new input information into the P2CCD circuit, these samples are read out, converted and shifted into the shift register.
Then for a period of about 5 ms zero information will be shifted into the P2CCD, controlled by the signal NUL IN from the ACL unit which is active in the vertical channels (see also 6.1.1.1.).
These zero information is then read out and corrected (see also 6.1.1.2.) with the 256 samples of signal information which was already stored in the shift register and the corrected information is shifted again in the shift register. This total procedure results then in a NDR pulse and copying of shift register contents into the ACCU memory can be started.

6.1.2. Display system

The display part consists of hardware to store and display data on the CRT display. Moreover this part arranges the coding for information to be displayed on pilot and control lamps and on the alphanumeric display. This chapter can be divided in:

6.1.2.1. Memories
6.1.2.2. Dot join and plot
6.1.2.3. Vertical amplifier
6.1.2.4. Horizontal amplifier
6.1.2.5. CRT section
6.1.2.6. Alphanumeric display

6.1.2.1. Memories (unit A6 page 6–61)

The memories are consisting of four separate parts which can be written and read independently. If from the acquisition control logic the signal New Data Ready arrives, new information is written in the ACCU.
This means that the contents of the shift register is copied in the ACCU.
This information is now read out continuously with a speed, determined so that the display on the CRT seams to be steady.
At a "SAVE" command the contents of the ACCU is copied in one or more of the registers STO1 . . . STO3.
The registers STO1 ... STO3 can only copy information from the ACCU. The only other possibility to write in one of the memories STO1 . . . STO3 is with the use of the IEC-bus interface via the databus.
The information is stored in the memories as a two-complement notation which means that the data are integers with values from −128 up to and including +127. To convert this in straight binary notation for the YDAC only the most significant bit has to be inverted. After that the complete information can be inverted by operating the push pull knobs "pull to invert". This inversion takes place by an eight-bit-exclusive-or.
Via the databus the information can be applied also to the X-DAC. This is necessary in the mode X = A; Y = B.

6.1.2.2. Dot join and plot (unit A20 page 6–178)

If the mode "DOTS" is selected separate dots will appear on the CRT display.
The dot join circuit generates straight lines between the consecutively dots. The block diagram of the dot join principle is shown in the figure below.

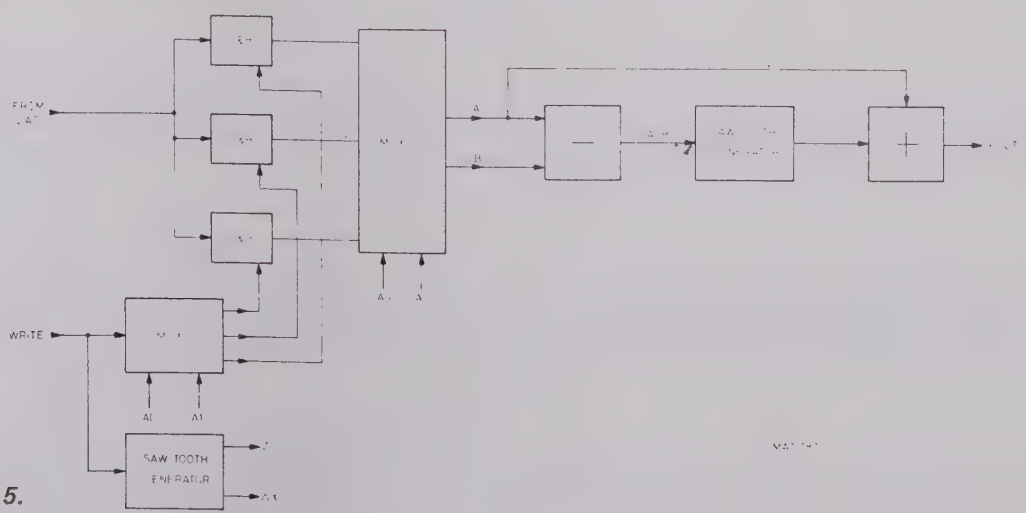


Fig. 6.1.5.

In dual channel operation on points 1 and 3 is always the information of one channel. By the control signals AØ and A1 this information is switched to the output of the multiplexer. Suggest A is the oldest information and B the newest, then, the subtractor output is A-B. This voltage controls the variable sawtooth generator of which the ramp is determined so that the B value is reached before a new write pulse arrives. The output of the sawtooth generator is added to the oldest information A and applied to the final amplifier.
If the sawtooth generator is reset the CRT display is blanked.
For X-deflection also a sawtooth voltage is generated but now with a fixed ramp and amplitude.
The plot action is principally a software matter.
The microprocessor system activates the sample and hold gates for the plots so that every 0.25 sec a new sample is taken. This is visible on the CRT display as an intensified point so it is traceable for how far the plot action is got.
The speedness is choosen in such a way that a simple chart recorder is able to record the information.

6.1.2.3. *Vertical amplifier (unit A20 page 6–178)*

After the dot join it is possible to magnify the signal 5x. Now it is possible to obtain the contents of the ACCU or STO1 ... STO3 for full screen deflection. In Y x 1 mode for each memory two divisions are available. Midrange of the position controls effects in displaying the memory base lines on the CRT at resp. 1, 3, 5 and 7 cm with respect to the screen top. This offset is switched to zero if the Y x 5 mode is choosen.
Now all base lines of the memories are situated in the centre of the screen.
The final amplifier consists of a long tailed pair which drives the CRT directly. This is possible because of the low bandwidth of 1 MHz.

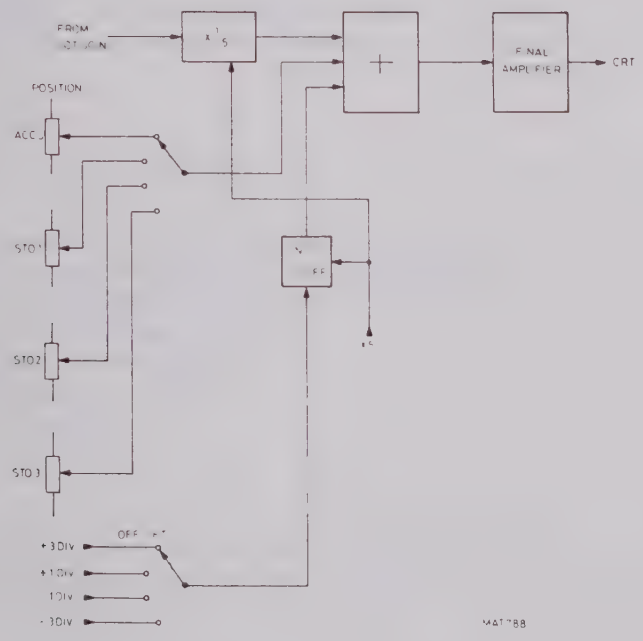


Fig. 6.1.6. DISPLAY CYCLE MUX

6.1.2.4. *Horizontal amplifier (unit A20 page 6–178)*

The horizontal amplifier consists of an integrated circuit for the magnifier adjusting and a final amplifier consisting of two shunted feedback pushpull amplifiers. Position control is effected at the input of the integrated circuit.

6.1.2.5. *CRT section (unit A15 page 6–157)*

Because of the principle of the CRT it is not necessary to correct the barrel and pin cushion distortion.
The cathode current of the CRT as used in the concept of this oscilloscope will never yet very high so that a focus voltage dependent to the intensity setting can be arranged automatically. Now there is no need for a front panel focus control.
The Z-control is arranged by the microprocessor system.
Only if a memory is read the CRT is unblanked.
If via the overflow detection a maximum or a minimum value is exceeded this part is displayed with a frequency of approx. 5 Hz so the display blinks.

6.1.2.6. *Display (unit A2 page 6–25)*

There are four front-panel alphanumeric displays:
- channel A V/DIV display
- channel B V/DIV display
- s/DIV display
- DIV display.

Each of these alphanumeric displays is an intelligent four-digit unit with a built-in CMOS integrated circuit. The integrated circuit contains a memory, an ASCII-character generator, and a LED multiplexing and drive circuit.

The displays are controlled by the microprocessor, each individual display section being selected by means of addresses fed to the ADDRESS-bus by the microprocessor.

The characters that are required to be displayed are generated by the microprocessor system in Standard ASCII character code and are placed on the databus (signals DØ ... D7).

Control and pilot lamps

The NOT TRIG'D, RUN and REMOTE lamps are directly controlled by the signals $\overline{\text{NOT TRIG'D}}$, $\overline{\text{RUNL}}$ and $\overline{\text{REM}}$, which are generated on the microprocessor board.

The DISPLAY lamps, the SELECT lamps, the UNCAL A and UNCAL B lamps, the A and B AMPL/DIV control lamps and the TIME/DIV control lamps are controlled by addresses generated by the microprocessor system.

6.1.3. **Microprocessor** (unit A4 page 6–45)

As shown in the simplified block diagram, the micro-processor unit basically consists of the following circuit elements:
- A micro-processor integrated circuit block for controlling and organising data flow.
- Ereasable and programmable read-only memories (EPROMs) for system programming.
- Random-access memories (RAMs) for stacking and storing the variable data.
- Address and data selection latches for the multiplexed address bus.
- Decoders for RAM and ROM selection and address decoding.
- Trap and watchdog circuits to guard against loss of data
- Two-way buffer circuit to the system data-bus.
- A blanking circuit for the c.r.t.

The heart of the microprocessor unit is an 8-bit microprocessor type 8085 with 16 address lines.
The first eight address lines AØ ... A7 are multiplexed with the eight data lines DØ ... D7 and are defined as ADØ ... AD7. Addressing is selected by the ALE (address latch enable) signal from the microprocessor, which gives an external indication when address information is on the bus-lines.

Trap Input Circuit

The TRAP input is effective when the battery back-up facility is used. It prevents the RAM contents being disturbed when the instrument is switched off or in the event of a power failure. The TRAP input forces the microprocessor to continue with the execution of the program at the starting address of the POWER DOWN routine. Failure of the power supply activates the TRAP input of the microprocessor.

A 5 MHz crystal, is connected to the clock inputs of the microprocessor to provide an accurate timing reference source.

A reset signal is generated when the instrument is switched ON. This reset signal forces the microprocessor to start the execution of the main program.

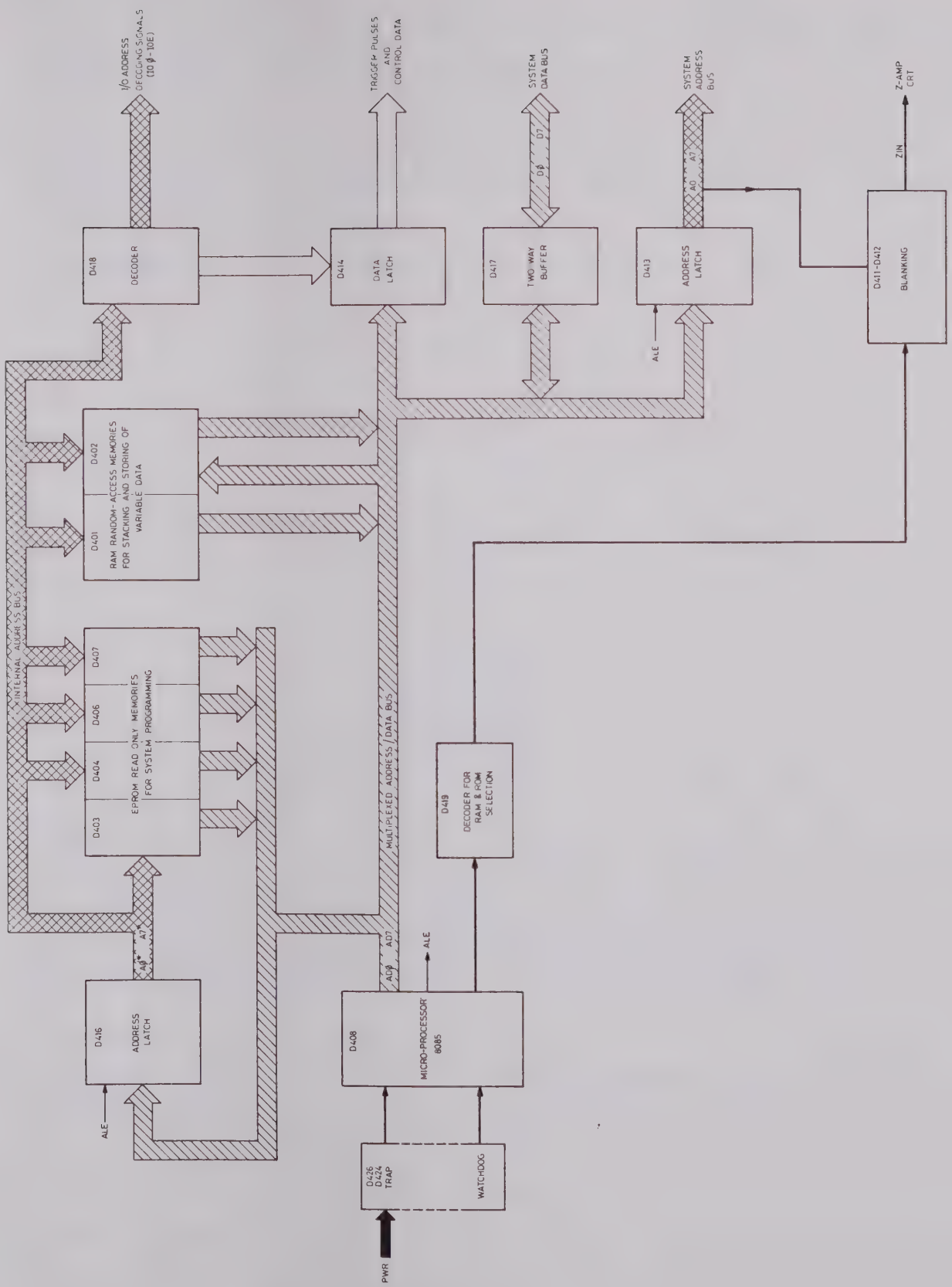


Fig. 6.1.7. Simplified block diagram microprocessor unit.

Connection to the system address bus

The first eight address bits placed by the microprocessor on the multiplexed address-data bus lines AD0 ... AD7 have to be separated from the eight data bits.
This separation is achieved by an address latch, which is enabled by signal ALE.
The group of output signals A0 ... A7 constitute the system address bus.

Connection to the system data-bus

The eight data bits placed by the microprocessor on the multiplexed address-data bus lines AD0 ... AD7 have to be separated from the first eight address bits.
This separation is done by a bidirectional buffer.

System memory map

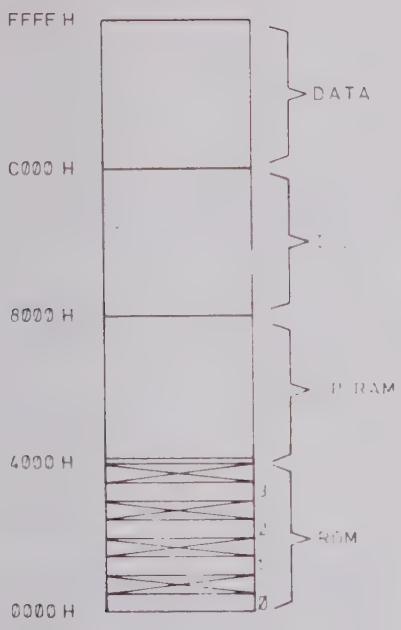


Fig. 6.1.8.

ROM memory

The ROM (read-only memory), which contains the system program, consists of the four EPROM chips of 2K-bytes each (2048X 8 bits).
Because the microprocessor's first eight address lines AD0 ... AD7 are multiplexed in the microprocessor with the data lines, the addresses have to be latched by the address latch D416 with the aid of the ALE signal.
When a certain ROM address is selected, the contents of the selected location are placed on the multiplexed address-data bus lines AD0 ... AD7.

RAM memory

The μP-RAM (microprocessor random access memory) is used by the microprocessor for stack purposes and for storage of variable data.
It consists of two RAM chips - of ¼ K-nibbles each (256 x 4 bits), which means that a maximum of 256 bytes of data can be stored.

Each μP-RAM memory address can be selected by the address lines A0* ... A7*

Reading the RAM contents or writing data into a RAM location is controlled by the signals $\overline{RD}$* and $\overline{WR}$*

The data to be written into, or read from the RAM memory is transported via the multiplexed address-data bus AD0 ... AD7.

Blanking circuit

This circuit provides for a blanking signal ZIN (Z-amplifier input) for blanking the trace on the c.r.t. display.

6.1.4. Power supply (unit A15 page 6–157 and A16 page 6–166)

The mains voltage is applied via the mains filter and the mains selector switch on the AC POWER UNIT A16 to a rectifier where it is full-wave rectified and fed to a regulated sine-converter (oscillator and switching circuit). The output voltage of the sine converter is kept constant by regulating the duty cycle of the applied voltage by a special integrated circuit.
This output voltage is applied to the primary of a transformer, the secundary voltages of this transformer are applied to DC POWER unit A15 where they are full-wave rectified, smoothed and applied to the various circuits. Also the voltages for the C.R.T. filament and the C.R.T. cathode (−1,5 kV) are generated here.
The −1.5 kV is also applied to the EHT unit A23 which gives a high tension for g8 of the C.R.T.

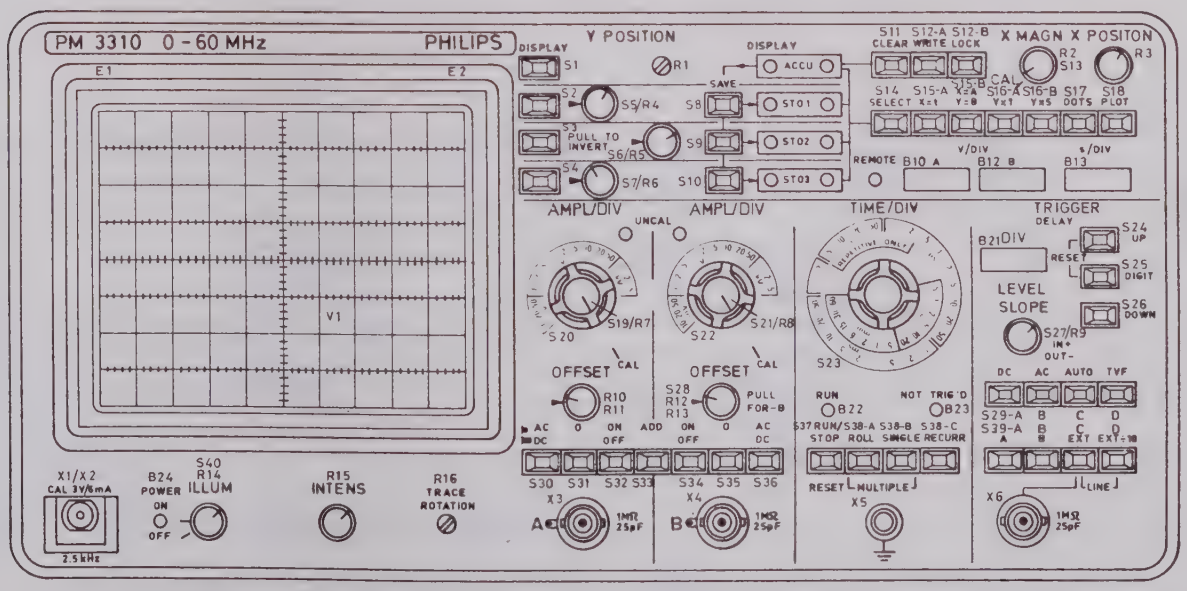
The MAINS triggering is taken direct from the mains and, via an opto-isolator, fed to the trigger circuitry on a safe level.

6.2. UNIT DESCRIPTIONS

6.2.1. Front side unit A1

The front side unit consists of an aluminium front cast on which the following items are mounted.

- LED B24 + LED-holder
- Light reflector assembly inclusive two lampholders and two 28 V - 80 mA lamps E1 and E2.
- CAL output terminals X1 and X2.
- Measuring earth socket X5.
- BNC input socket X6 for external triggering.
- LEVEL/SLOPE control R9/S27.
- INTENS control R15.
- TRACE ROTATION control R16.
- Trigger mode selector switch S29.



MAT 708A

Fig. 6.2.1.

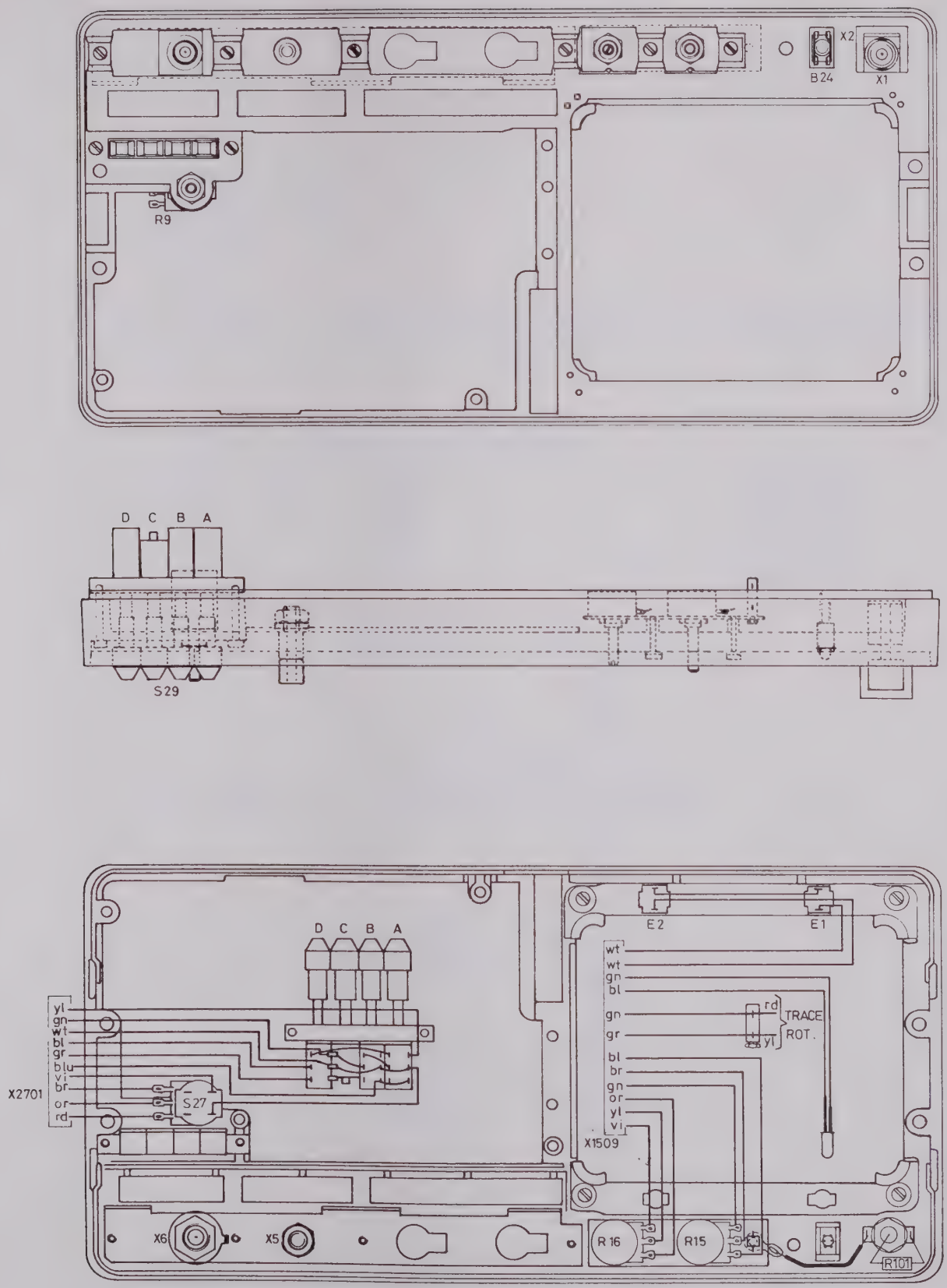


Fig. 6.2.2.

MAT 707A

6.2.2. Front unit A2

6.2.2.1. Front board A201

The front board houses all the front-panel control lamps, pilot lamps and alphanumeric displays.

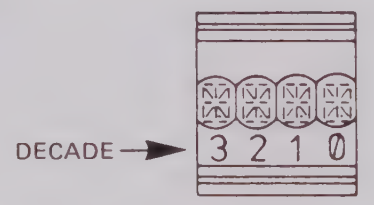
Alphanumeric intelligent displays

There are four front-panel alphanumeric displays:
- channel A V/DIV display
- channel B V/DIV display
- s/DIV display
- DIV display

Each of these alphanumeric displays is an intelligent four-digit unit with a built-in CMOS integrated circuit. The integrated circuit contains a memory, an ASCII-character generator, and a LED multiplexing and drive circuit.

The displays are controlled by the microprocessor, each individual display section being selected by means of addresses fed to the ADDRESS-bus by the microprocessor.

DECADE	A0	A1
0	0	0
1	0	1
2	1	0
3	1	1



A V/DIV display

DECADE	CONTROL ADDRESS
0	80A0
1	80A1
2	80A2
3	80A3

B V/DIV display

DECADE	CONTROL ADDRESS
0	80A4
1	80A5
2	80A6
3	80A7

s/DIV display

DECADE	CONTROL ADDRESS
0	80A8
1	80A9
2	80AA
3	80AB

DIV display

DECADE	CONTROL ADDRESS
0	80AC
1	80AD
2	80AE
3	80AF

The characters that are required to be displayed are generated by the microprocessor system in Standard ASCII character code and are placed on the data-bus (signals D0 ... D7).

CHARACTER SET
(all other input codes
display 'BLANK')

CHARACTER SET

D6 D5 D4 D3 \ D2 D1 D0	L L L	L L H	L H L	L H H	H L L	H L H	H H L	H H H
L H L L		!	"	#	$	%	&	'
L H L H	(	)	*	+	,	-	.	/
L H H L	0	1	2	3	4	5	6	7
L H H H	8	9	:	;	<	=	>	?
H L L L	@	A	B	C	D	E	F	G
H L L H	H	I	J	K	L	M	N	O
H L H L	P	Q	R	S	T	U	V	W
H L H H	X	Y	Z	[	\	]	^	_

Control and pilót lamps

The NOT TRIG'D, RUN and REMOTE lamps are directly controlled by the signals $\overline{\text{NOT TRIG'D}}$, $\overline{\text{RUNL}}$, and $\overline{\text{REM}}$, which are generated on the microprocessor board.

The DISPLAY lamps (DISØ ... DIS3), the SELECT lamps (SELØ ... SEL3), the UNCAL A and UNCAL B lamps, the A and B AMPL/DIV control lamps LA1, LA1Ø, LB1, LB1Ø and the TIME/DIV control lamps LREC - LROLL are controlled by the addresses 8ØBØ and 8ØB4 as shown in the table in conjunction with the data bits DØ to D7.

ADDRESS	D7	D6	D5	D4	D3	D2	D1	DØ
8ØBØ	SEL3	SEL2	SEL1	SELØ	DIS3	DIS2	DIS1	DISØ
8ØB4	UNCB	UNCA	LROLL	LREC	LB1Ø	LB1	LA1Ø	LA1

Selection of a display segment or a group of pilot lamps or control lamps is achieved by decoder D203.
This three-bit decoder decodes the three address-bits A2, A3 and A4 if the input signal combination WR.I0A is active. This results in one active decoder output line at a time.
The I0A signal is an address decoding signal for address lines A5 ... A15 and decodes addresses 8ØAØ to 8ØBF.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	DESCRIPTION
A0		A4	Address bits from system address bus
A1		A4	
A2		A4	
A3		A4	
A4		A4	
D0		A4	Data bits from system data-bus
D1		A4	
D2		À4	
D3		A4	
D4		A4	
D5		A4	
D6		A4	
D7		A4	
$\overline{\text{NOT TRIG'D}}$		A4	Control for NOT TRIG'D lamp
$\overline{\text{IOA}}$		A4	Address decoding signal for addresses 80A0H - 80FFH (Display select)
$\overline{\text{REM}}$		A4	Control for REMOTE lamp
$\overline{\text{RUNL}}$		A4	Control for RUN lamp
$\overline{\text{WR}}$		A4	Signal WRITE from microprocessor
+5 V		A15	
		A15	

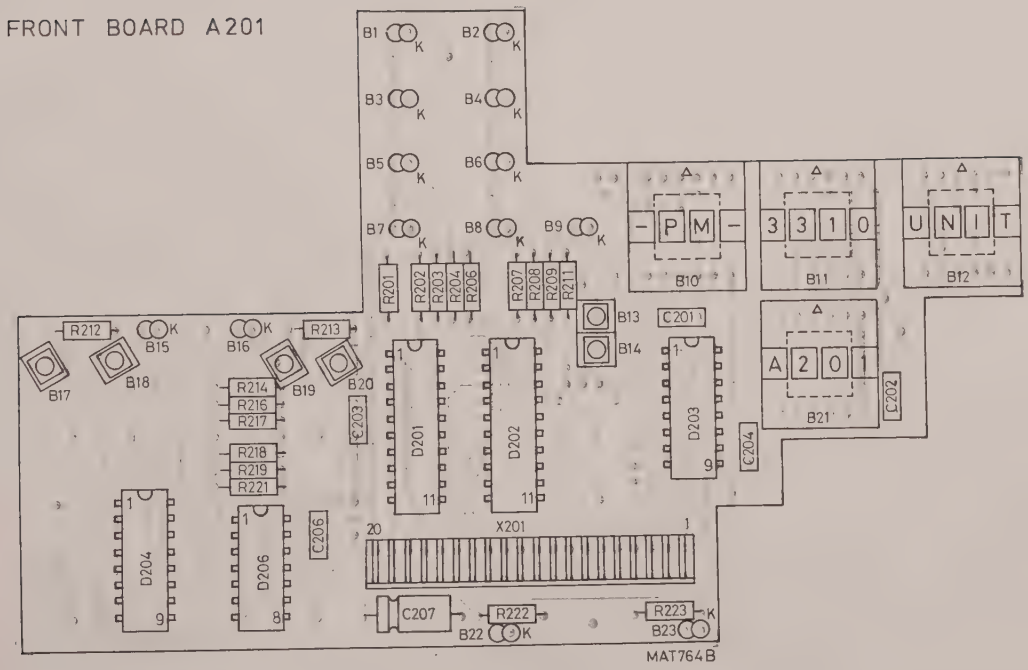
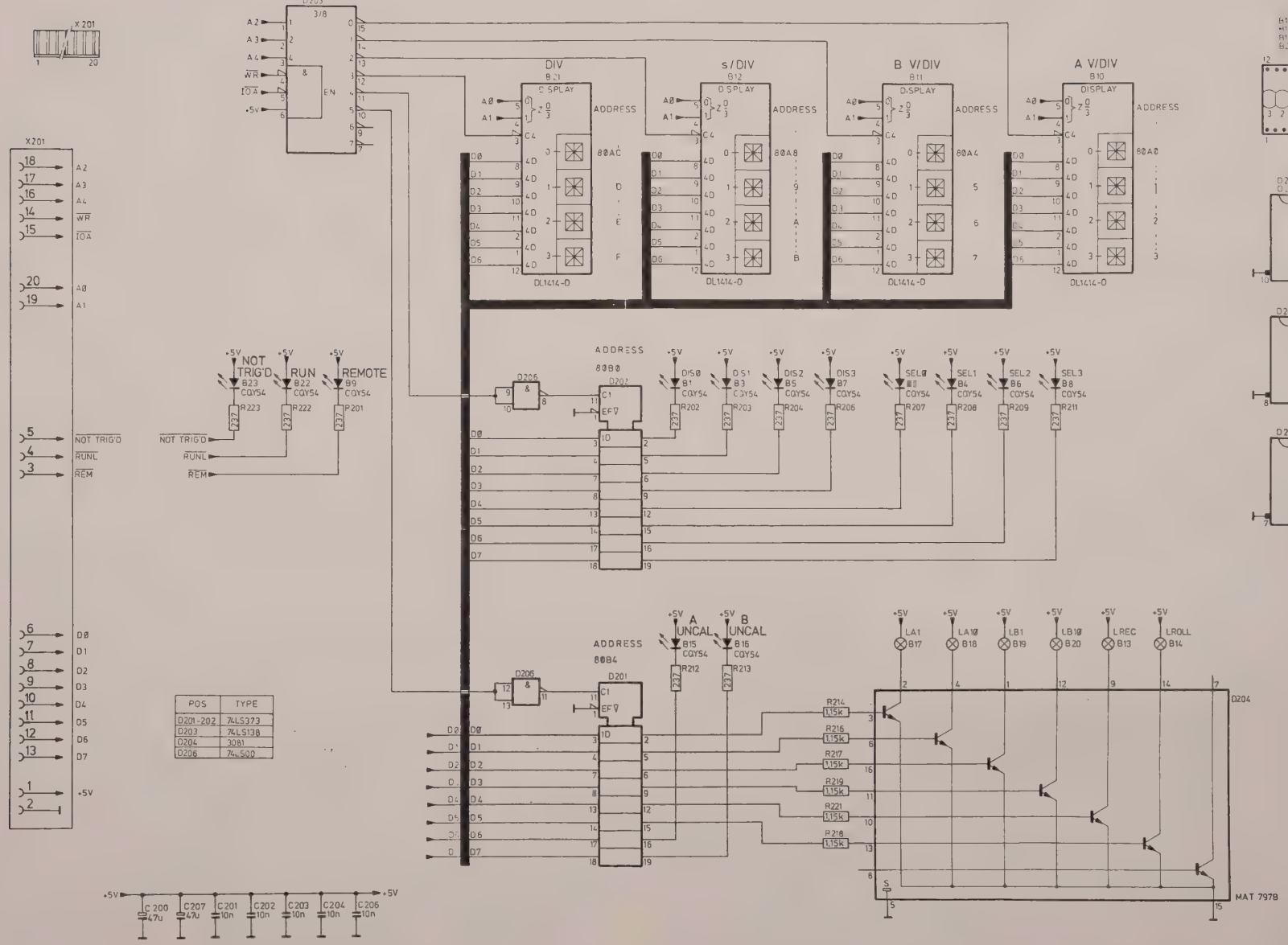

FRONT BOARD A201
B1
B2
B3
B4
B5
B6
B7
B8
B9
K
– P M –
B10
3 3 1 0
B11
U N I T
B12
R201
R202
R203
R204
R206
R207
R208
R209
R211
B13
B14
C201
R212
B15
B16
R213
B17
B18
B19
B20
R214
R216
R217
R218
R219
R221
C203
D201
D202
D203
A 2 0 1
B21
C202
C204
D204
D206
C206
20
X201
1
C207
R222
B22
R223
B23
MAT764B

Fig. 6.2.3.



POS	TYPE
D201-202	74LS373
D203	74LS138
D204	3081
D206	74LS00

Fig. 6.2.4.

6.2.2.2. Switchboard A202 and Switch Units A203 ... A207

The front-panel controls listed below are located on these units.

A202 switchboard

SWITCHES	Circuit ref.	Switch signals
YA AMPL/DIV	S20	YA1, YA2, YA4, YA5, YA6, YA7 — See table A
YB AMPL/DIV	S22	YB1, YB2, YB4, YB5, YB6, YB7 — See table B
TB TIME/DIV	S23	TB1, TB2, TB4, TB5, TB6, TB7 — See table C
INV STO1	S5	$\overline{\text{INV1}}$
INV STO2	S6	$\overline{\text{INV2}}$
INV STO3	S7	$\overline{\text{INV3}}$
CAL A	S19	$\overline{\text{CALA}}$
CAL B	S21	$\overline{\text{CALB}}$
INV YB	S28	$\overline{\text{BIN}}$
SERV 1	X241	$\overline{\text{SERV1}}$
SERV 2	X241	$\overline{\text{SERV2}}$

POTENTIOMETERS	Circuit ref.	Slider signals
X POSITION	R3	X POS
X MAGN	R2	X MAGN (+12 V in X CAL)
OFFSET A	R10/R11	OFF A
OFFSET B	R12/R13	OFF B
POS ACCU	R1	POSØ
POS STO1	R4	POS1
POS STO2	R5	POS2
POS STO3	R6	POS3
CONT A	R7	ACON
CONT B	R8	BCON

The slider signals of the above-listed potentiometers are applied to various units of the instrument via connector X259

A203 interconnection board

Provides the connection between units S201 and A202.

A204 display switch board

		Switch signals
DISPLAY ACCU	S1	$\overline{DIS\emptyset}$
DISPLAY STO1	S2	$\overline{DIS1}$
DISPLAY STO2	S3	$\overline{DIS2}$
DISPLAY STO3	S4	$\overline{DIS3}$

A 205 I *delay switch board*

UP ┐ RESET	S24	$\overline{UP}$
DIG ┘	S25	$\overline{DIG}$
DOWN	S26	$\overline{DOWN}$

A 205 II *save switch board*

SAVE STO1	S8	$\overline{SAV1}$
SAVE STO2	S9	$\overline{SAV2}$
SAVE STO3	S10	$\overline{SAV3}$

A206 clear switch board

CLEAR	S11	$\overline{CLEAR}$
WRITE	S12A	–
LOCK	S12B	$\overline{LOCK}$

A207 select switch board

SELECT	S14	$\overline{SEL}$
X=t	S15A	–
X=A/Y=B	S15B	$\overline{A/B}$
Yx1	S16A	–
Yx5	S16B	$\overline{Yx5}$
DOTS	S17	$\overline{DOTS}$
PLOT	S18	$\overline{PLOT}$

The settings of all the switches on the above units are read periodically by the microprocessor system via three groups of multiplexers, D241/D247, D242/D248, D243/D249 according to the following table:

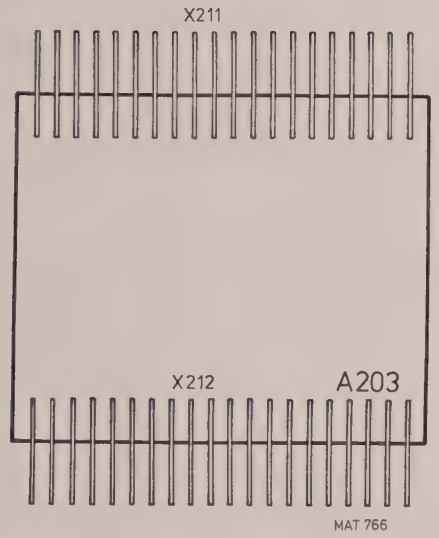
ADDRESS		A0F	D7	D6	D5	D4	D3	D2	D1	D0
8020	$\overline{RDF\emptyset}$=0	1	YA1	YA4	YA5	YA6	YA7	YA2	$\overline{DIG}$	$\overline{CALA}$
8021	$\overline{RDF\emptyset}$=0	0	YB1	YB4	YB5	YB6	YB7	YB2	$\overline{BIN}$	$\overline{CALB}$
8022	$\overline{RDF2}$=0	1	TB1	TB4	TB5	TB6	TB7	TB2	$\overline{UP}$	$\overline{DOWN}$
8023	$\overline{RDF2}$=0	0	$\overline{DIS3}$	$\overline{DIS2}$	$\overline{DIS1}$	$\overline{DIS\emptyset}$	$\overline{INV3}$	$\overline{INV2}$	$\overline{INV1}$	FRUN
8024	$\overline{RDF4}$=0	1	+5 V	FASA	$\overline{Yx5}$	$\overline{SEL}$	$\overline{SAV3}$	$\overline{SAV2}$	$\overline{SAV1}$	DELTRG
8025	$\overline{RDF4}$=0	0	$\overline{PLOT}$	0 V	$\overline{DOTS}$	$\overline{A/B}$	$\overline{CLEAR}$	$\overline{LOCK}$	$\overline{SERV2}$	$\overline{SERV1}$

The selection of one of the multiplexer groups and the internal setting of the selected group is made via the address selector circuit, which consists of NAND-gate D244 (11, 12, 13) and the three-to-eight decoder circuit D246, as shown in the following table:

ADDRESS	$\overline{IO2}$	A3	A2	A1	AØ	AØF
8Ø2Ø	Ø	Ø	Ø	Ø	Ø	1
8Ø21	Ø	Ø	Ø	Ø	1	Ø
8Ø22	Ø	Ø	Ø	1	Ø	1
8Ø23	Ø	Ø	Ø	1	1	Ø
8Ø24	Ø	Ø	1	Ø	Ø	1
8Ø25	Ø	Ø	1	Ø	1	Ø

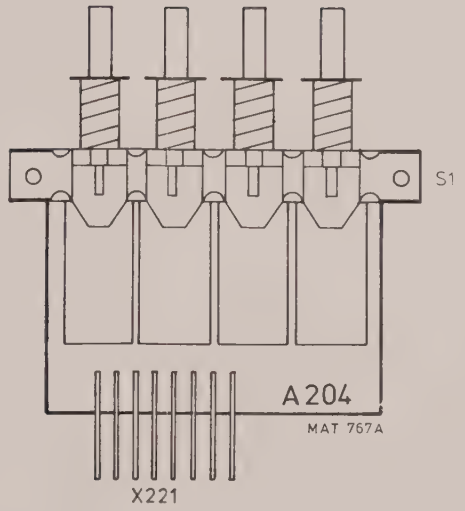
INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A0 ... A4		A4		Address bits from system address-bus
	ACON	A202	A21	Slider of channel A continuous control
	BCON	A202	A21	Slider of channel B continuous control
D0 ... D7		A4		Data bits from system data-bus
	D0 ... D7	A202	A4	Data bits to system data-bus
DELTRG		A13	A9	Delayed trigger signal
FASA		A9		Output phase flip-flop
FRUN		A13		Freerun signal
$\overline{IO2}$		A4		Input switches select } I/O address decoding signals
$\overline{IOA}$		A4		Display select } I/O address decoding signals
NOT TRIG'D		A4		Control for NOT TRIG'D lamp
	OFFA	A202	A21	Slider of channel A OFFSET control
	OFFB	A202	A21	Slider of channel B OFFSET control
	POSØ	A202	A20	Slider of ACCU position control
	POS1	A202	A20	Slider of STO1 position control
	POS2	A202	A20	Slider of STO2 position control
	POS3	A202	A20	Slider of STO3 position control
$\overline{REM}$		A4		Control for REMOTE lamp
$\overline{RUNL}$		A4		Control for RUN lamp
$\overline{RD}$		A4		Signal READ from microprocessor
$\overline{WR}$		A4		Signal WRITE from microprocessor
	XMAG	A202	A20	Slider of XMAGN control
	XPOS	A202	A20	Slider of X POSITION control
+5 V		A15		
−12 K		A15		
+12 K		A15		
−12 L		A15		
+12 L		A15		
⏚		A15		

TEST POINTS	
X248	DØ
X249	D1
X251	D4
X252	D5



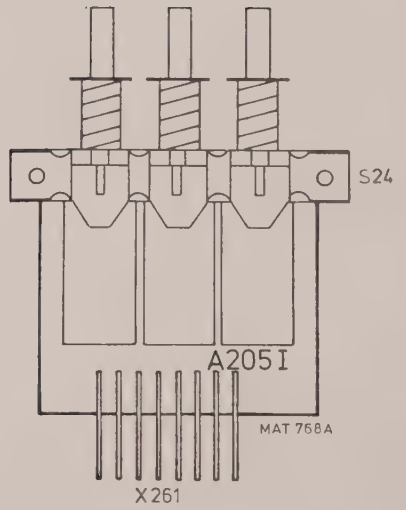
INTERCONNECTION BOARD

Fig. 6.2.5.



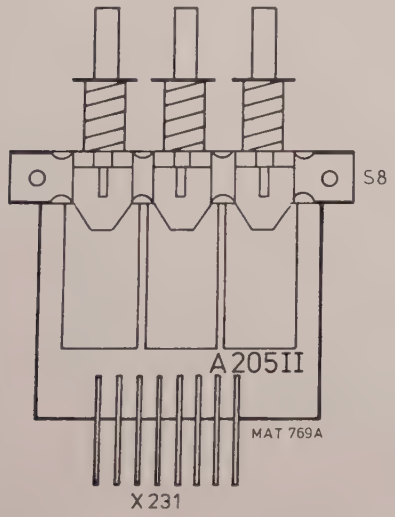
DISPLAY SWITCH BOARD

Fig. 6.2.6.

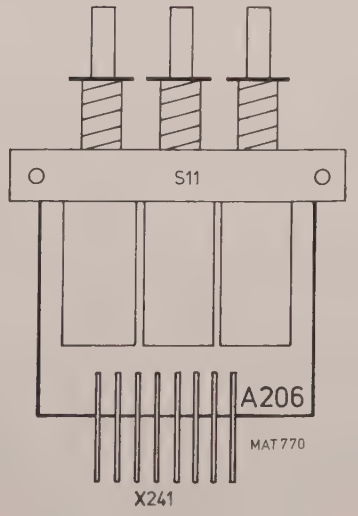


DELAY SWITCH BOARD

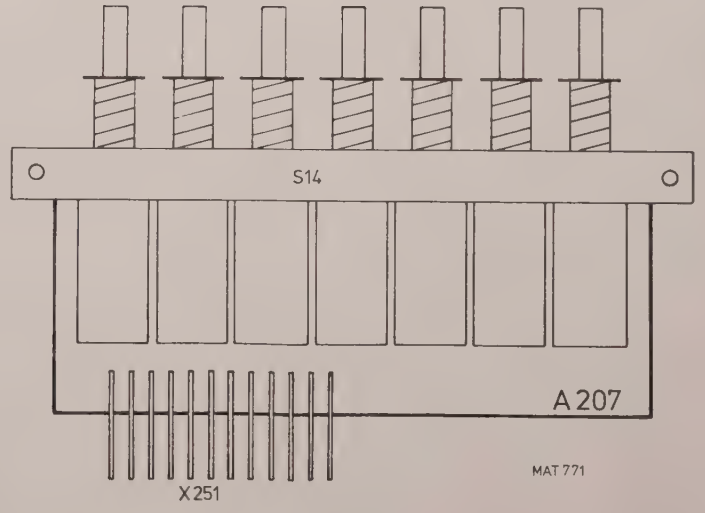
Fig. 6.2.7.



SAVE SWITCH BOARD



CLEAR SWITCH BOARD



SCALE SWITCH BOARD

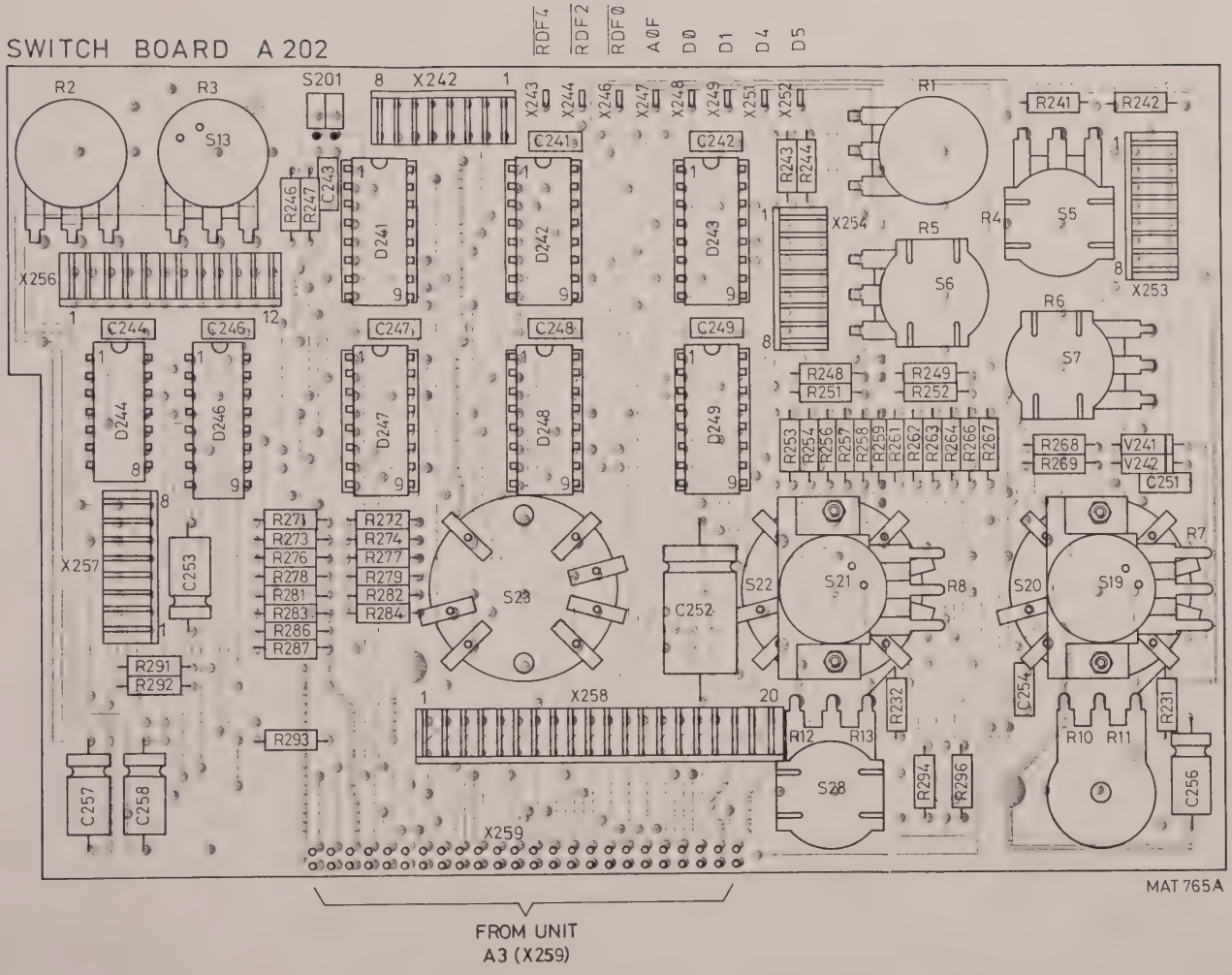
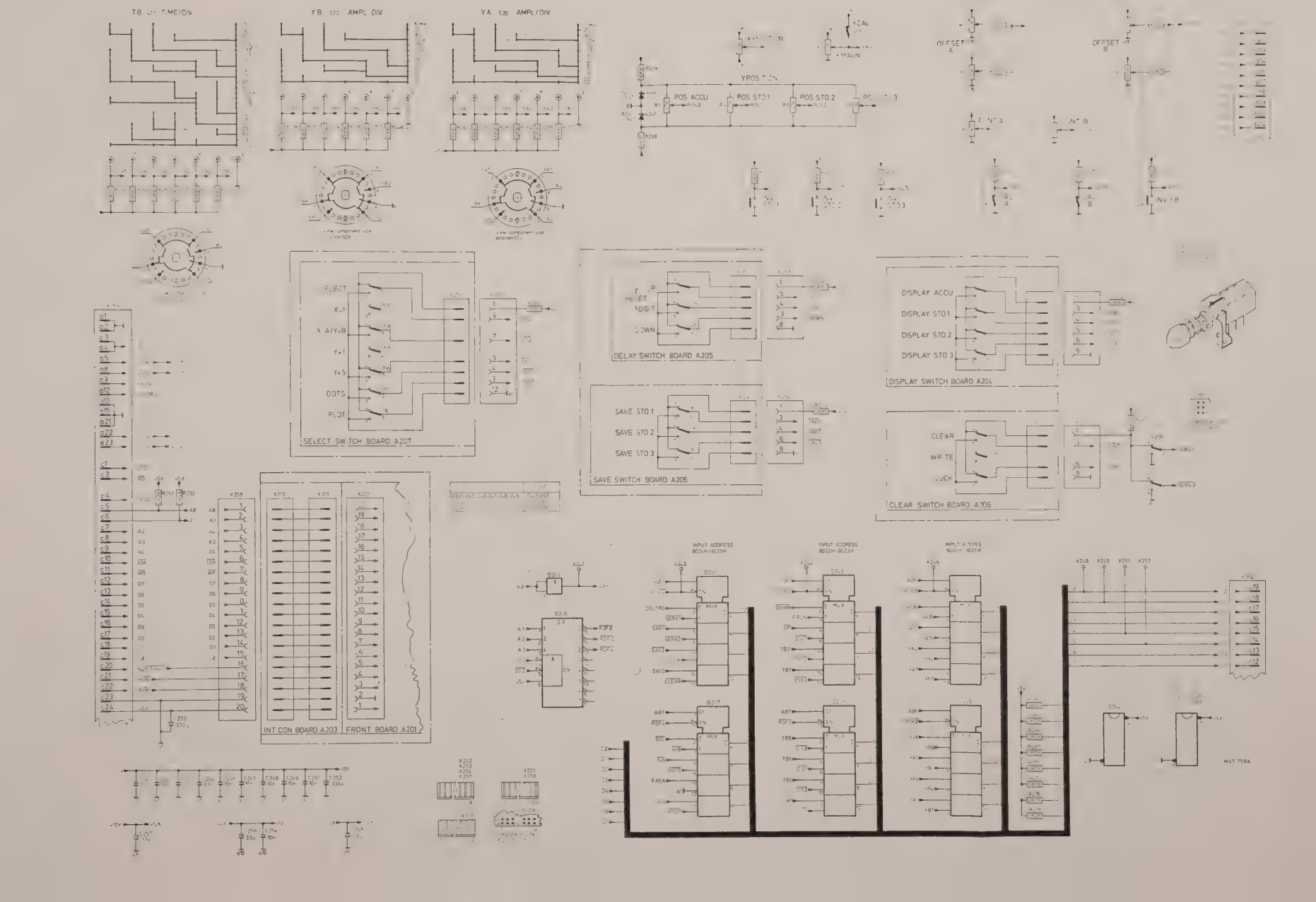

SWITCH BOARD A 202
RDF4
RDF2
RDF0
A0F
D0
D1
D4
D5
S201
X242
X243
X244
X246
X247
X248
X249
X251
X252
R1
R2
R3
S13
R241
R242
C241
C242
R243
R244
X254
R4
S5
X253
X256
D241
D242
D243
R5
S6
R6
S7
C244
C246
C247
C248
C249
D244
D246
D247
D248
D249
R248
R249
R251
R252
R253
R254
R256
R257
R258
R259
R261
R262
R263
R264
R266
R267
R268
R269
V241
V242
C251
X257
C253
R271
R272
R273
R274
R276
R277
R278
R279
R281
R282
R283
R284
R286
R287
S23
C252
S22
S21
R8
S20
S19
R7
R291
R292
X258
R293
R12
R13
R232
S28
R294
R296
C254
R231
R10
R11
C256
C257
C258
X259
MAT 765A
FROM UNIT
A3 (X259)

Fig. 6.2.11.


TB TIME/DIV
YB AMPL/DIV
YA AMPL/DIV
POS ACCU
POS STO1
POS STO2
OFFSET A
OFFSET B
SELECT
X-1
X A/Y+B
Y+1
Y+5
DOTS
PLOT
SELECT SWITCH BOARD A207
DELAY SWITCH BOARD A205
SAVE STO1
SAVE STO2
SAVE STO3
SAVE SWITCH BOARD A205
DISPLAY ACCU
DISPLAY STO1
DISPLAY STO2
DISPLAY STO3
DISPLAY SWITCH BOARD A204
CLEAR
CLEAR SWITCH BOARD A206
INT CON BOARD A203
FRONT BOARD A201
INPUT ADDRESS 8020H/8025H
INPUT ADDRESS 8022H/8023H
INPUT ADDRES 9020H-9021H
MAT 708A

6.2.3. Motherboard unit A3

The motherboard unit is installed to interconnect the various plug-in units.
No components are mounted on this board.

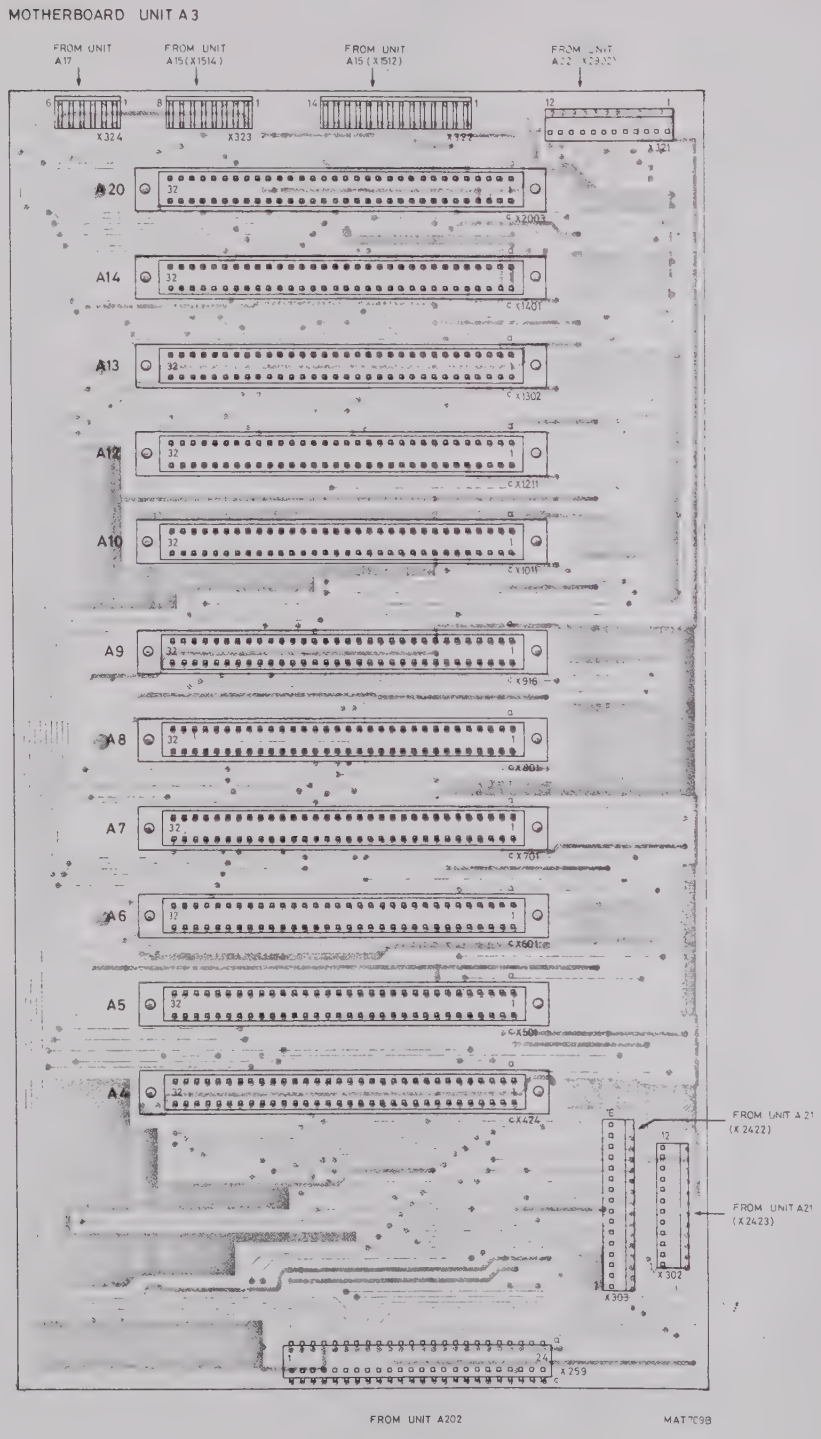


Fig. 6.2.13.

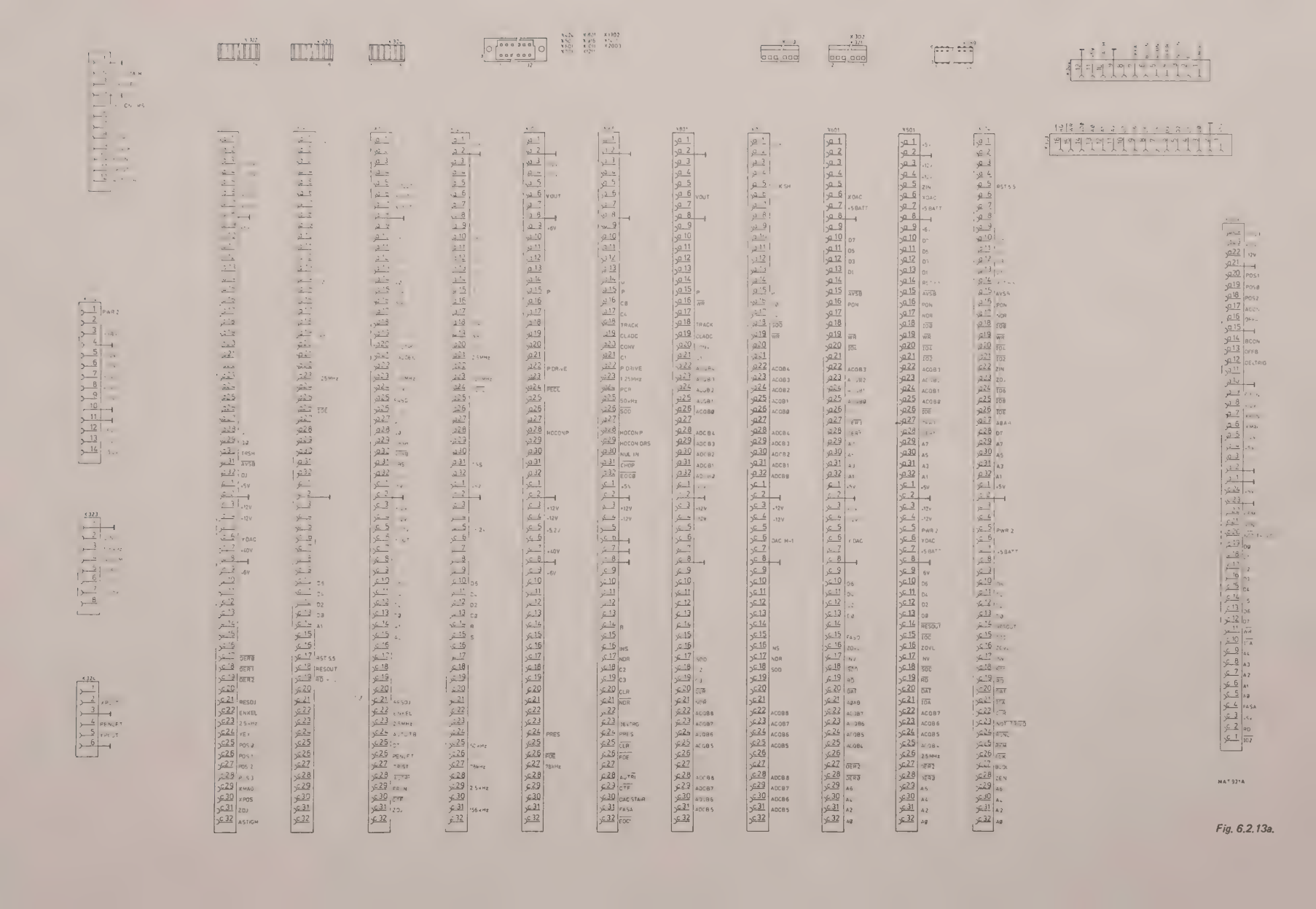


Fig. 6.2.13a.

6.2.4. Microprocessor unit A4

6.2.4.1. General

As shown in the simplified block diagram, the microprocessor unit basically consists of the following circuit elements:

- A microprocessor integrated circuit block for controlling and organising data flow.
- Erasable and programmable read-only memories (EPROMs) for system programming.
- Random-access memories (RAMs) for stacking and storing the variable data.
- Address and data selection latches for the multiplexed address bus.
- Decoders for RAM and ROM selection and address decoding.
- Trap and watchdog circuits to guard against loss of data.
- Two-way buffer circuit to the system data-bus.
- A blanking circuit for the c.r.t.

The heart of the microprocessor unit is integrated circuit D408, an 8-bit microprocessor type 8085 with 16 address lines.
The first eight address lines AØ ... A7 are multiplexed with the eight data lines DØ ... D7 and are defined as ADØ ... AD7. Addressing is selected by the ALE (address latch enable) signal from the microprocessor, which gives an external indication when address information is on the bus-lines.

6.2.4.2. Trap Input Circuit

The TRAP input is effective when the battery back-up facility is used. It prevents the RAM contents being disturbed when the instrument is switched off or in the event of a power failure. The TRAP input can be regarded as a non-maskable restart input. A logic 1 level on this input forces the microprocessor to continue with the execution of the program starting at address ØØ24H, the starting address of the POWER DOWN routine.

The signal PWR (power), a 50Hz sinewave signal generated on the power supply unit, is converted to a 50Hz squarewave voltage on pin 3 of Schmitt trigger D426 and integrated by C437/R412 to provide pulses on input 11 of the retriggerable one-shot D424.

During the initial switching-on of the power supply, a low voltage on reset input 13 of the one-shot holds the circuit in its reset state. When the power supply is started, however, the retriggerable one-shot switches over and signal PON (power on) goes to logic 1. As long as pulses are generated on input 12, the one-shot will remain in this state.

Failure of the power supply, i.e. no control pulses on input 11, causes the one-shot to be reset and thus activate the TRAP input of the microprocessor.
For test procedures, the circuit can be isolated by unsoldering the spot on the printed-circuit track.

6.2.4.3. CLOCK inputs X_1 and X_2

A 5 MHz crystal, B401, is connected to the clock inputs X_1 and X_2 of the microprocessor to provide an accurate timing reference source.

6.2.4.4. $\overline{RESIN}$ input and WATCHDOG Circuit

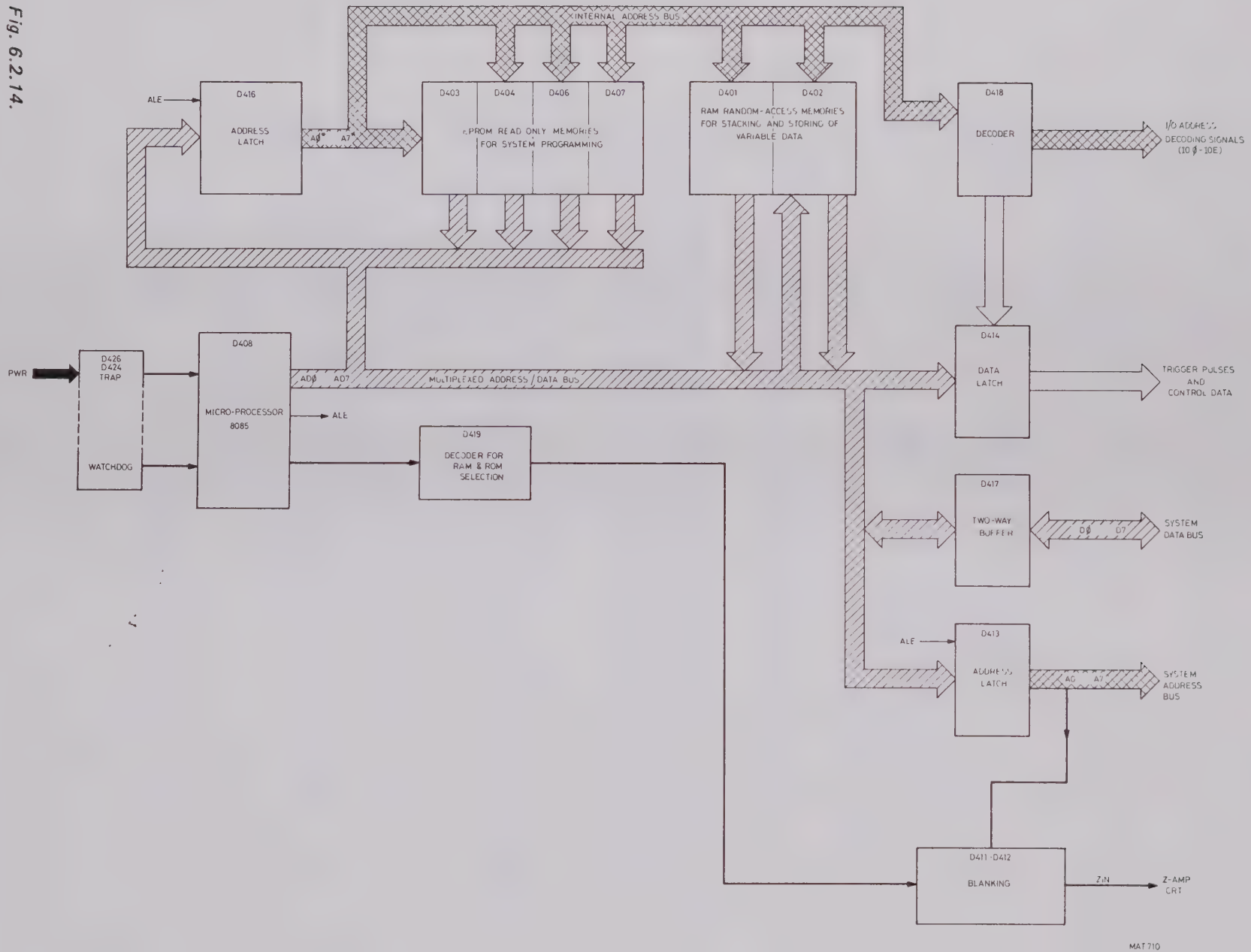
A reset signal is generated when the instrument is switched ON. This reset signal forces the microprocessor to start the execution of the main program beginning at the address ØØØØH.

The retriggerable one-shot D424 is initially reset by input pin 3 (R) during the switching-on of the instrument. After switching on, the one-shot is set to the logic 1 state by the DT (display timing) pulses from the display timing flip-flop D409, pin 9 on this p.c. board, applied to D424-5.

The one-shot remains in this state as long as the system continues to generate DT pulses.

If these pulses are interrupted, the circuit functions as a watchdog and resets the microprocessor. The one-shot will in fact be reset to logic 0 and a 1 Hz Schmitt oscillator consisting of C432/V402/R421 and D426 will switch the $\overline{RESIN}$ input of the microprocessor between logic 0 and logic 1.

Fig. 6.2.14.


INTERNAL ADDRESS BUS
ALE
D416
ADDRESS LATCH
A0 A7
D403 D404 D406 D407
EPROM READ ONLY MEMORIES FOR SYSTEM PROGRAMMING
D401 D402
RAM RANDOM-ACCESS MEMORIES FOR STACKING AND STORING OF VARIABLE DATA
D418
DECODER
I/O ADDRESS DECODING SIGNALS (IO 0 - IOE)
PWR
D426 D424 TRAP
WATCHDOG
D408
MICRO-PROCESSOR 8085
ALE
AD0 AD7
MULTIPLEXED ADDRESS / DATA BUS
D419
DECODER FOR RAM & ROM SELECTION
D414
DATA LATCH
TRIGGER PULSES AND CONTROL DATA
D417
TWO-WAY BUFFER
D0 D7
SYSTEM DATA BUS
ALE
D413
ADDRESS LATCH
A0 A7
SYSTEM ADDRESS BUS
D411 - D412
BLANKING
Z-IN
Z-AMP CRT
MAT 710

This reset process continues unless the program resumes correct running.

For test purposes, the watchdog circuit can be replaced by a fixed reset circuit by soldering the spot on the printed-circuit track.

6.2.4.5. RST 7.5 – RST 6.5 – RST 5.5 inputs

These restart inputs to the microprocessor force it to continue the program on defined addresses, from where it can jump to different programs.

RESTART INPUTS	PRIORITY	RESTART ADDRESS	REMARKS
RS 7.5	Highest	ØØ3CH	Not used in standard instruments (can eventually be used for test purposes)
RS 6.5		ØØ34H	Not used in standard instruments (connected to 'SPARE' connector)
RS 5.5	Lowest	ØØ2CH	Used by IEC-bus interface option

6.2.4.6. SID (Serial data input)

The microprocessor will receive the information NDR (new data ready) on the SID input.

6.2.4.7. READY input

Via this input, additional WAIT states are generated to double the $\overline{RD}$* and $\overline{WR}$* pulse duration. This is necessary to provide correct adaption between the microprocessor and the slower acting data RAM circuits.
The length of the signals $\overline{RD}$* and $\overline{WR}$* is doubled by flip-flop D423 only when signal $\overline{DAT}$ is logic 0.
The output of this flip-flop D423 is connected to the microprocessor READY input to indicate the end of the wait time.

6.2.4.8. Connection to the system address bus

The first eight address bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the eight data bits. This separation is achieved by address latch D413, which is enabled by signal ALE.
The group of output signals AØ ... A7 constitute the system address bus.

6.2.4.9. Connection to the system data-bus

The eight data bits placed by the microprocessor on the multiplexed address-data bus lines ADØ ... AD7 have to be separated from the first eight address bits.
This separation is done by the bidirectional buffer D417.
This buffer is selected if address line A15 is logic 1 (as in I/O and DATA part of the memory map).
Input or output data depends on the logic level of signal RD*.

RD* = logic 1 means OUTPUT
RD* = logic 0 means INPUT

Data is transported between the D417 in- and outputs and the system data-bus over the lines DØ ... D7.

SYSTEM MEMORY MAP

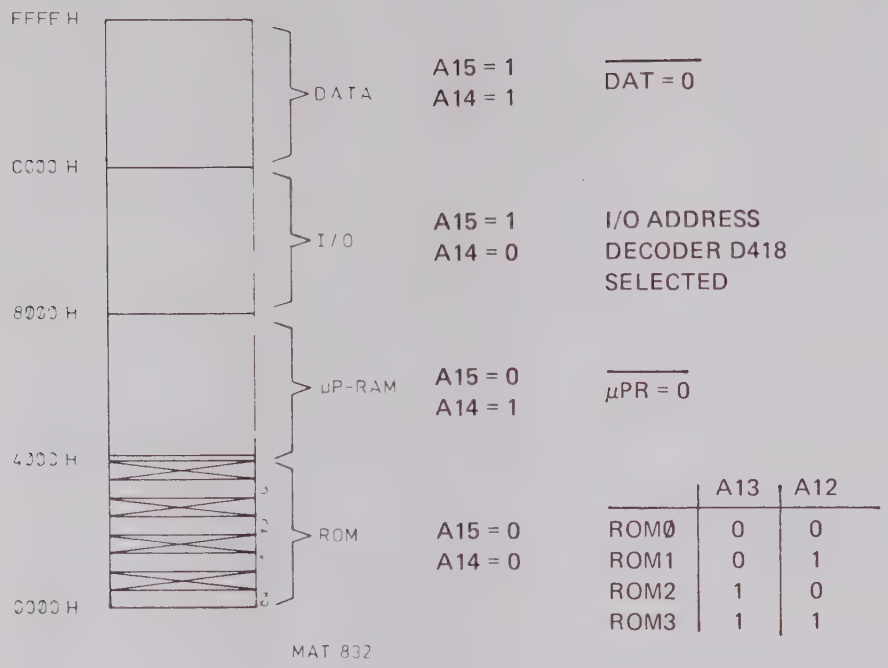


Fig. 6.2.15.

ADDRESS DECODING

6.2.4.10. ROM - µP/RAM - I/O - DATA selection

In decoder D419, four select signals are generated as follows:

A15	A14	OUTPUT SIGNAL
0	0	ROM selection to pin 15 - D419
0	1	µPRAM selection signal $\overline{UPR}$
1	0	I/O selection signal (not used)
1	1	DATA SELECTION SIGNAL $\overline{DAT}$

ROM chip select signals ROMØ ... ROM3

A15	A14	A13	A12	OUTPUT SIGNAL	ADDRESSES
0	0	0	0	$\overline{ROMØ}$	ØØØØ - Ø7FF
0	0	0	1	$\overline{ROM1}$	1ØØØ - 17FF
0	0	1	0	$\overline{ROM2}$	2ØØØ - 27FF
0	0	1	1	$\overline{ROM3}$	3ØØØ - 37FF

I/O select signals $\overline{IOØ}$ ... $\overline{IOE}$.

The three-bit decoder D418 decodes the address bits A15, A14, A7*, A6* and A5* into the eight address decoding signals $\overline{IOØ}$ ... $\overline{IOE}$. Each of these signals represent a group of addresses as shown in the table. The signals are used in various circuits of the instrument.

A15	A14	A7*	A6*	A5*	OUTPUT SIGNAL	ADDRESSES	TO UNIT
1	0	0	0	0	$\overline{IO0}$	8000 - 801F	A21 AMPLIFIER
1	0	0	0	1	$\overline{IO2}$	8020 - 803F	A2-A4 SWITCHES + µP
1	0	0	1	0	$\overline{IO4}$	8040 - 805F	A6 RAM
1	0	0	1	1	$\overline{IO6}$	8060 - 807F	A12 TIME-BASE
1	0	1	0	0	$\overline{IO8}$	8080 - 809F	A13 TRIGGER DELAY
1	0	1	0	1	$\overline{IOA}$	80A0 - 80BF	A2 DISPLAY
1	0	1	1	0	$\overline{IOC}$	80C0 - 80DF	NOT USED
1	0	1	1	1	$\overline{IOE}$	80E0 - 80FF	A14 IEC OPTION

ROM MEMORY

The ROM (read-only memory), which contains the system program, consists of the four EPROM chips D403 - D404 - D406 and D407 and 2K-bytes each (2048X 8 bits).

Because the microprocessor's first eight address lines AD0 ... AD7 are multiplexed in the microprocessor with the data lines, the addresses have to be latched by the address latch D416 with the aid of the ALE signal. The ALE signal enables the latching of the A0* ... A7* signals. These A0* ... A7* signals are placed on the microprocessor board internal address bus.

Each ROM memory address can be selected by the address lines A0* ... A7* together with address lines A8 - A9 and A10.

Each ROM memory chip is selected by the read signal $\overline{RD}$* and the relevant ROM selection signal $\overline{ROM0}$, $\overline{ROM1}$, $\overline{ROM2}$ or $\overline{ROM3}$.

When a certain ROM address is selected in this way, the contents of the selected location are placed on the multiplexed address-data bus lines AD0 ... AD7.

µP-RAM MEMORY

The µP-RAM (microprocessor random access memory) is used by the microprocessor for stack purposes and for storage of variable data.
It consists of two RAM chips D401 - D402 of ¼K-nibbles each (256 x 4 bits), which means that a maximum of 256 bytes of data can be stored.

Each µP-RAM memory address can be selected by the address lines A0* ... A7*.
The two chips are selected by the signal combination PON.UPR.

Reading the RAM contents or writing data into a RAM location is controlled by the signals $\overline{RD}$* and $\overline{WR}$*.

The data to be written into, or read from the RAM memory is transported via the multiplexed address-data bus AD0 ... AD7.

DATA LATCH D414

When the microprocessor places the address 8020 on the multiplexed address data bus, this results in signal $\overline{IO2}$ going to logic 0. This $\overline{IO2}$ combined with the $\overline{WR}$ signal on gate D421 enables data latch D414 to latch the byte of data present on the multiplexed address data-bus.

The byte of data consists of the following signals:

BIT 0	$\overline{CLR}$	Clear signal for clearing the shift register
BIT 1	$\overline{REM}$	Control signal for REMOTE lamp
BIT 2	$\overline{NOT\ TRIG'D}$	Control signal for NOT TRIG'D lamp
BIT 3	$\overline{ZEN}$	Z enable signal
BIT 4	$\overline{RUNL}$	Control signal for RUN lamp
BIT 5	BLOL	Blinking overload signal
BIT 6	INV	Invert signal for RAM output data
BIT 7	CLDT	Clear display timing flip-flop

BLANKING CIRCUIT

This circuit provides for a blanking signal ZIN (Z-amplifier input) for blanking the trace on the c.r.t. display.

ZIN = logic 1 means blanking.

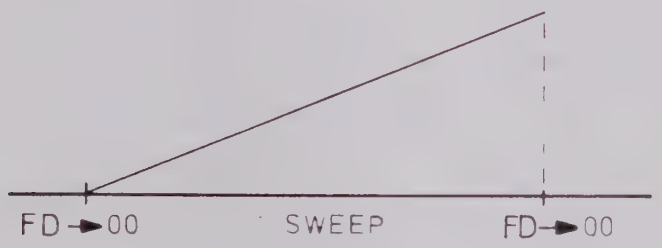
The trace on the c.r.t. display is only present if all the input signals of NAND circuit D411 are logic 1 at the same time.

– pin 4 The signal ZEN is only present during the time that a selected memory (ACCU, STO1, STO 2 or STO3) is displayed.

– pin 11 If an overflow is detected on the RAM unit the short signal ZOVL (Z-overflow), will be latched in a D-type flip-flop D423 with the clock signal DAT.WR.
As the output signal of the flip-flop is connected to OR circuit D421, the blinking overload signal is passed to pin 11 of the NAND D411, resulting in blinking of the trace at a low frequency.

– pin 3 In mode DOTS, the ZDJ (Z dot join) blinking signal will be active.

– pin 5 Signal DT (display timing) blanks the trace when no memory contents (ACCU, STO1, STO2 or STO3) are displayed. Signal DT is derived from the addresses, which are also applied to the XDAC for horizontal deflection.



NAND circuit D412 detects the address FDH on the first eight address lines.
The output signal indicates the beginning and the end of a sweep by going to logic 1 level. This signal is latched in D-type flip-flop D409 with the clock signal DAT.WR, resulting in a signal DT.
The trace is blanked if DT = logic 0. Flip-flop D409 can be reset by signal CLDT (clear display timing flip-flop) resulting in a blanked trace.

– pin 1 In mode X = A/Y = B (A versus B – AVSB)
a signal ZAB is generated on output pin 5 of flip-flop D409.
Data can only be latched in this flip-flop on clock signal DAT.WR.
This data is derived from signal AØAB.
(AØAB is address AØ in mode X = A/Y = B)

TRIGGER PULSES FOR TEST PURPOSES

Trigger pulse 'START MAINLOOP' is available at X407
Trigger pulse "START DISPLAY LOOP" is available at X409
Trigger pulse 'START DELAY LOOP' is available at X412

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	A0 ... A7	A4		Address bits from system address bits
A0AB		A6		Address bit A0 in X = A/Y = B mode
$\overline{\text{AVSB}}$		A13	A6	Logic 0 in X = A/Y = B mode
	BLOL	A4		Blinking overload
	$\overline{\text{CLK}}$	A4		Microprocessor clock pulse output signal (2,5 MHz
	$\overline{\text{CLR}}$	A4	A8–A9	Clear signal for shift register
D0 ... D7	D0 ... D7	A4-A6		Data bits from system data-bus
	$\overline{\text{DAT}}$	A4	A6	Data selection
	DT	A4	A13	Display timing
	INV	A4	A6	Signal invert
	$\overline{\text{IO0}}$	A4	A21	Input switches select amplifier settings (A21)
	$\overline{\text{IO2}}$	A4	A202	Input switches select (A2) Output port select (A4)
	$\overline{\text{IO4}}$	A4	A6	Data RAM select (A6)
	$\overline{\text{IO6}}$	A4	A12	Time-base select (A12)
	$\overline{\text{IO8}}$	A4	A13	Delay trigger unit settings (A13)
	$\overline{\text{IOA}}$	A4	A201/A202	Display select (A2)
	$\overline{\text{IOC}}$	A4	NOT USED	
	$\overline{\text{IOE}}$	A4	A14	

I/O address decoding signals.

NDR		A9		New data ready
	$\overline{\text{NOT TRIG'D}}$	A4	A201/A202	Control for NOT TRIG'D lamp
	PON	A4	A6	Power on
PWR		A15		Power signal (20 kHz)
	$\overline{\text{RD}}$	A4		Signal READ from microprocessor
	$\overline{\text{REM}}$	A4	A201/A202	Control for REMOTE lamp
	$\overline{\text{RESOUT}}$	A4	A14	Microprocessor RESET OUTPUT signal
RST5,5		A14		Restart 5,5 input from IEC-bus interface
RST6,5		A5		Restart 6,5 input (not used)
	$\overline{\text{RUNL}}$	A4	A201/A202	Control for RUN lamp
	$\overline{\text{SOD}}$	A4	A6–7–9	Microprocessor serial output data
	$\overline{\text{WR}}$	A4		Signal WRITE from microprocessor
ZDJ		A13		Z dot join
	ZEN	A4		Z enable
	ZIN	A4	A15	Z input
ZOVL		A6		Z overflow signal
+5 V		A15		
		A15		
+5 BATT		A15		

TEST POINTS	
X401	D421-pin 6 (WR.DAT)
X402	PON
X403	$\overline{\text{UPR}}$
X404	DT
X406	$\overline{\text{ROMØ}}$
X407	$\overline{\text{REM}}$
X408	$\overline{\text{ROM1}}$
X409	$\overline{\text{RUNL}}$
X411	$\overline{\text{ROM2}}$
X412	$\overline{\text{NOT TRIG'D}}$
X413	$\overline{\text{ROM3}}$
X414	ALE
X416	A15
X417	NDR
X418	SOD
X419	$\overline{\text{RD}}$*
X421	CLK (OUT)
X422	$\overline{\text{WR}}$*
X423	

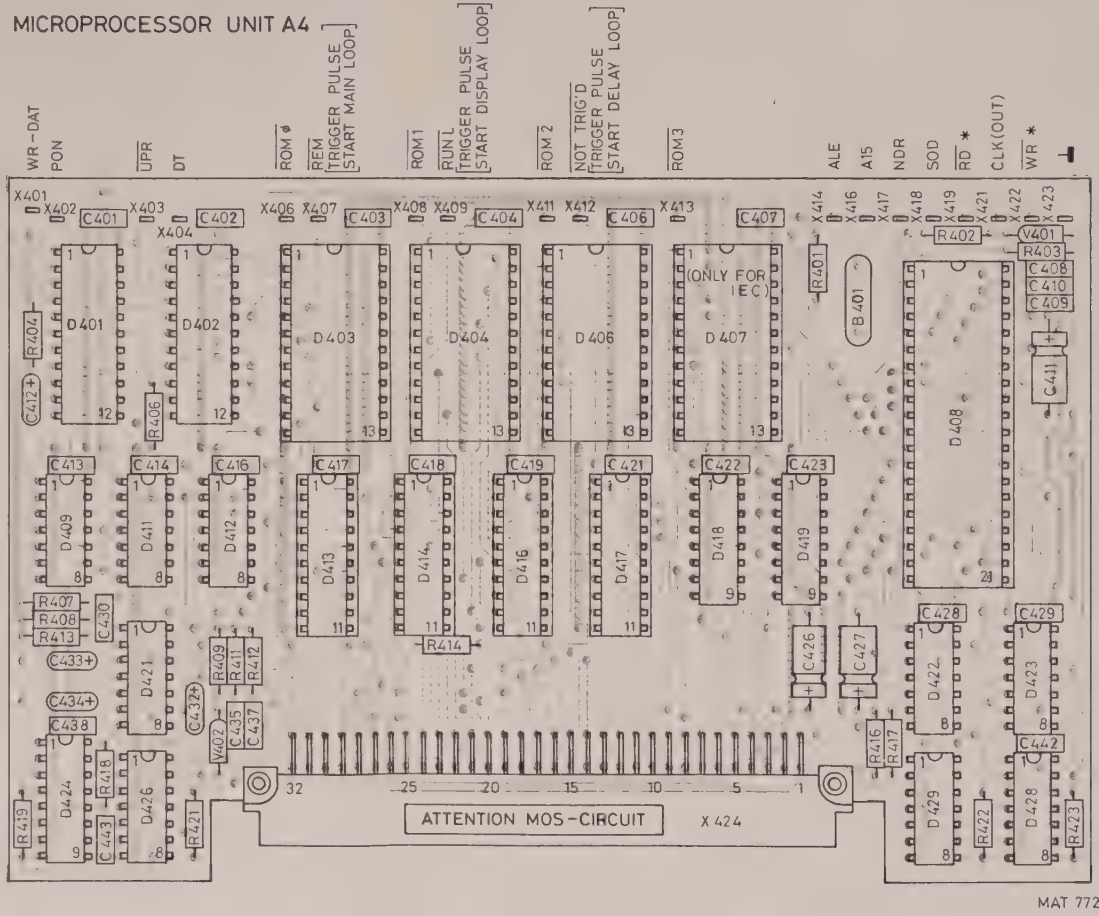

MICROPROCESSOR UNIT A4
WR-DAT
PON
UPR
DT
ROM Ø
REM TRIGGER PULSE START MAIN LOOP
ROM 1
RUN L TRIGGER PULSE START DISPLAY LOOP
ROM 2
NOT TRIG'D TRIGGER PULSE START DELAY LOOP
ROM3
ALE
A15
NDR
SOD
RD *
CLK(OUT)
WR *
(ONLY FOR IEC)
ATTENTION MOS-CIRCUIT
X 424
MAT 772 B

Fig. 6.2.16.

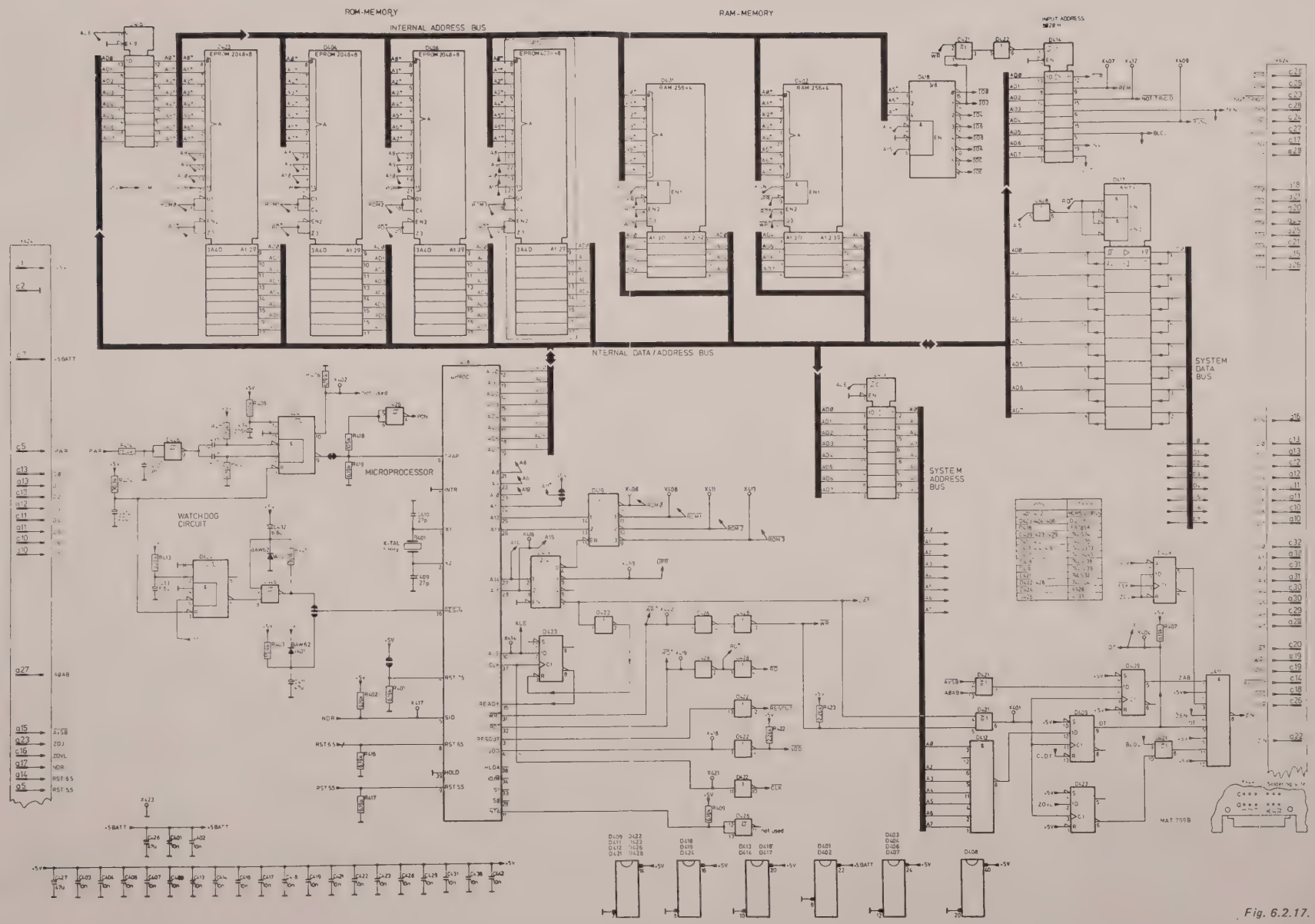

ROM-MEMORY
RAM-MEMORY
INTERNAL ADDRESS BUS
INTERNAL DATA/ADDRESS BUS
EPROM 2048×8
RAM 256×4
INPUT ADDRESS
SYSTEM DATA BUS
SYSTEM ADDRESS BUS
MICROPROCESSOR
WATCHDOG CIRCUIT
MAT 799B

Fig. 6.2.17.

6.2.5. Spare unit A5

There is a connector X501 available on the motherboard unit A3 in which no plug-in unit is placed.

On this connector X501 a number of signals are available for measuring purposes.

A1	+5 V	C1	+5 V
A2	0 V	C2	0 V
A3	+12 V	C3	+12 V
A4	−12 V	C4	−12 V
A5	ZIN	C5	PWR2
A6	XDAC	C6	YDAC
A7	+5 BATT	C7	+5 BATT
A8	0 V	C8	0 V
A9	+6 V	C9	−6V
A10	D7	C10	D6
A11	D5	C11	D4
A12	D3	C12	D2
A13	D1	C13	DØ
A14	RST 6.5	C14	$\overline{\text{RES OUT}}$
A15	$\overline{\text{AVSB}}$	C15	$\overline{\text{IOC}}$
A16	PON	C16	ZOVL
A17	NDR	C17	INV
A18	$\overline{\text{IOØ}}$	C18	$\overline{\text{SOD}}$
A19	$\overline{\text{WR}}$	C19	$\overline{\text{RD}}$
A20	$\overline{\text{IO4}}$	C20	$\overline{\text{DAT}}$
A21	$\overline{\text{IO2}}$	C21	$\overline{\text{IOA}}$
A22	ACQB3	C22	ACQB7
A23	ACQB2	C23	ACQB6
A24	ACQB1	C24	ACQB5
A25	ACQBØ	C25	ACQB4
A26	$\overline{\text{IOE}}$	C26	2,5 MHz
A27	$\overline{\text{OER3}}$	C27	$\overline{\text{OER2}}$
A28	$\overline{\text{OER1}}$	C28	$\overline{\text{OERØ}}$
A29	A7	C29	A6
A30	A5	C30	A4
A31	A3	C31	A2
A32	A1	C32	AØ

6.2.6. RAM unit A6

The RAM unit basically comprises the four random-access memories, ACCU, STO1, STO2, STO3 used for signal storage, the two digital-to-analog converters X DAC and Y DAC and their associated control circuits.

6.2.6.1. RAM memories ACCU, STO1, STO2, STO3

Each of the RAM memories consists of two RAM IC-chips of ¼K-nibbles each (256x4 bits) enabling a maximum of 256 bytes to be stored.

The overall memory is selected by PON.DAT = 1, i.e. with the power on and the data field addressed.
Memory allocation is as follows:

MEMORY	IC ELEMENTS
ACCU	D601, D602
STO1	D603, D604
STO2	D606, D607
STO3	D608, D609

Selection of one or more of the memories is made under microprocessor control.
A byte of data representing the information for reading or writing one or more of the memories is sent by the microprocessor on data-lines DØ ... D7 to the latch D613. If the signal combination WR.IO4 is logic 1, the data byte will be latched by D613.
Two groups of output signals are produced by latch D613:

Output Enable RAM signals (OER) – signals $\overline{\text{OER}}$Ø ... $\overline{\text{OER3}}$ select the memory of which the contents are required to be read.

Write Enable RAM signals (WRER) – signals $\overline{\text{WRER}}$Ø ... $\overline{\text{WRER3}}$ select the memory in which data is required to be written. With no WR signal available these signals are blocked.

Individual RAM locations are selected by address lines AØ ... A7.

Data inputs for the memories

Data received from other units can only be stored in the ACCU RAM.
Data stored in any of the other three memories STO1, STO2, STO3, is always derived from the ACCU memory.

Data for storage in the ACCU memory (D601, D602) can be:

- output data ACQBØ ... ACQB7 from the acquisition circuit,
- data from the microprocessor,
- data from the IEC-bus interface board via the system data-bus lines DØ ... D7.

The signals ACQBØ ... ACQB7 are applied to the latch D614 and the signals DØ ... D7 are applied to the latch D616.
Selection of either one of these latches is made under microprocessor control via the logic level of signal $\overline{\text{SOD}}$ (serial output data).

$\overline{\text{SOD}}$ = 1 selects D614
$\overline{\text{SOD}}$ = 0 selects D616 via inverter D626

Inverter D626 prohibits the output of data from both latches to the ACCU bit lines at the same time.

Overflow detection

The information in the RAMs is stored in 2's complement notation, which means that signal amplitudes are stored in positive as well as negative binary numbers.

maximum positive	+127	0111 1111
	⋮	⋮
	+1	0000 0001
	+0	0000 0000
	−1	1111 1111
	⋮	⋮
maximum negative	−128	1000 0000

From the above, we can see that if the most-significant bit of a binary number is at logic 0, we have a positive number, otherwise it represents a negative number.

An incorrect setting of the AMPL/DIV switch or the OFFSET control causes an overflow, which means that the result after digitising is greater than can be stored. Therefore, if the maximum number 0111 1111 or the minimum number 1000 0000 is reached, an overflow situation is recognised. This is signalled by a flashing trace on the c.r.t. display.

These two extreme overflow situations can be decoded as follows:

The most-significant bit D7 is inverted by D626 (1,2) resulting in the overflow codes 0000 0000 or 1111 1111. By comparing the inverted most-significant bit with the other seven bits in exclusive OR circuits D618 and D619, an output signal ZOVL (Z Overload) is indicated when one of these two overload situations occurs. The overflow signal ZOVL is applied to the Z-pulse (ZIN) circuit on Unit 4 to produce the flashing of the display when overload is reached.

6.2.6.2. *Digital-to-analog converters X DAC, Y DAC*

DAC output signals in X = t mode

Horizontal deflection on the c.r.t. display in the X = t mode is controlled by the addresses needed for reading the contents of the memories. Therefore, the address bits AØ ... A7 are applied to the X DAC (horizontal digital-to-analog converter) D622 to generate an analog deflection signal XDAC that varies between +5 V and −5 V.
The address bits are applied to the X DAC (D622) via two multiplexers D611 and D612, which are controlled by the signal $\overline{AVSB}$.

$\overline{AVSB}$ = 1 selects X = t mode
$\overline{AVSB}$ = 0 selects X = A / Y = B mode

Vertical deflection on the c.r.t. display is controlled by the eight data bits DØ' ... D7', which are applied to the Y DAC (D621) to generate an analog deflection signal Y DAC.
These data bits are routed to the Y DAC via eight exclusive OR gates D623, D624, which are controlled by the INV signal to invert the data when the front-panel INV switches are operated.

The X DAC and Y DAC latches can be enabled by the enable signals $\overline{X\ DACE}$ and $\overline{Y\ DACE}$ respectively. These are the output signals from the multiplexer D628, which is enabled by the $\overline{DAT}$ signal. Selection of input signals to the multiplexer is made by the signals AØAB and $\overline{AVSB}$ according to the following table:

$\overline{AVSB}$	AØAB	$\overline{XDACE}$	$\overline{YDACE}$	
0	0	WR	▬	X=A/Y=B mode
0	1	▬	WR	
1	0	WR	WR	X=t mode
1	1	WR	WR	

DAC output signals in X = A/Y = B mode

If channel A as well as channel B information is stored in the RAMs, XY deflection can be obtained by selecting the X = A/Y = B mode by depressing the relevant front-panel switch.
To give XY deflection, the channel information on A and B has to be applied to the X DAC and the Y DAC respectively.
There are two different methods of storing the channel A and channel B information in the RAMs.

Channel A ODD: (FASDI = 0) — Channel A information is stored in locations with ODD addresses and channel B in locations with EVEN addresses.

Channel A EVEN: (FASDI = 1) — Channel A information is stored in locations with EVEN addresses and channel B in locations with ODD addresses.

To obtain XY deflection, it is necessary to apply data from the ODD addresses to the X DAC and data from the EVEN addresses to the Y DAC or vice versa depending on the logic level of the FASDI signal.

For correct functioning, only one DAC latch may be enabled at a time, this being controlled by the enable signals $\overline{\text{XDACE}}$ and $\overline{\text{YDACE}}$ on the output of multiplexer D628.

The logic level of signal FASDI (phase of display) controls which channel is stored in odd or even addresses by determining which DAC is loaded first. If FASDI is at logic 0, we have the situation where X DAC (latch D622) is loaded first; i.e. channel A will be stored in the odd addresses.
Alternatively, if FASDI is at logic 1, then Y DAC (latch D621) will be loaded first and channel B will be stored in the odd addresses.

FASDI	AØ	AØAB
0	0	1
0	1	0
1	0	0
1	1	1

FASDI = 0 results in AØ being inverted
FASDI = 1 results in AØ not inverted

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A0 ... A7		A4		Address bits from system address bus
	A0AB	A6	A4	Address bit A0 in X=A/Y=B mode
ACQB0 ... ACQB7		A7		Acquisition output bits 0 ... 8
$\overline{\text{AVSB}}$		A13		Logic 0 in X=A/Y=B mode
D0 ... D7	D0 ... D7	A4-A6		Data bits from system data-bus
$\overline{\text{DAT}}$		A4		Data selection
FASDI		A13		Phase on display level
INV		A4		Signal invert
$\overline{\text{IO4}}$		A4		Data RAM select
	$\overline{\text{OER0}}$	A6	A20	Output enable RAM0
	$\overline{\text{OER1}}$	A6	A20	Output enable RAM1
	$\overline{\text{OER2}}$	A6	A20	Output enable RAM2
	$\overline{\text{OER3}}$	A6		Output enable RAM3
PON		A4		Power on
$\overline{\text{RD}}$		A4		Signal READ from microprocessor
$\overline{\text{SOD}}$		A4		Microprocessor serial output data
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
	X DAC	A6	A20	Horizontal DAC output signal
	Y DAC	A6	A20	Vertical DAC output signal
	ZOVL	A6	A4	Z overflow signal
+5 V		A15		
		A15		
+5 BATT		A15		
+12 V		A15		
−12 V		A15		

RAM UNIT A6

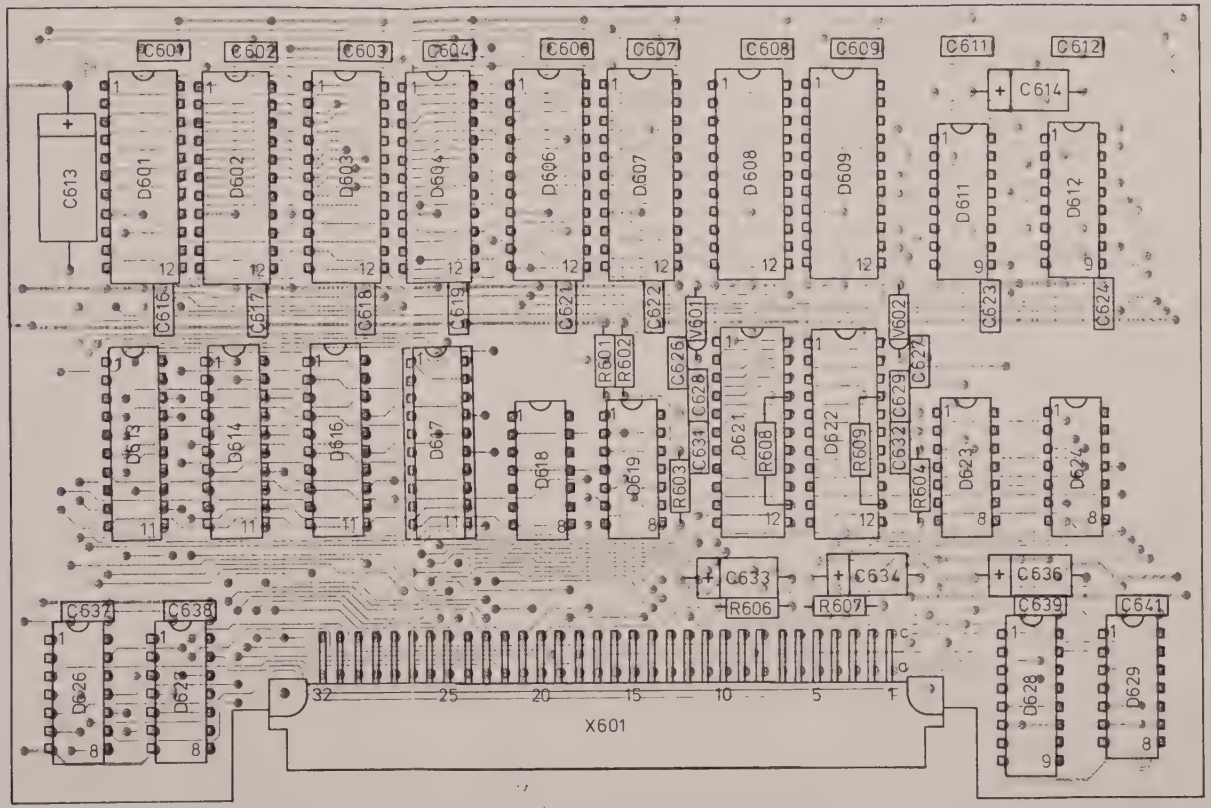


Fig. 6.2.18.

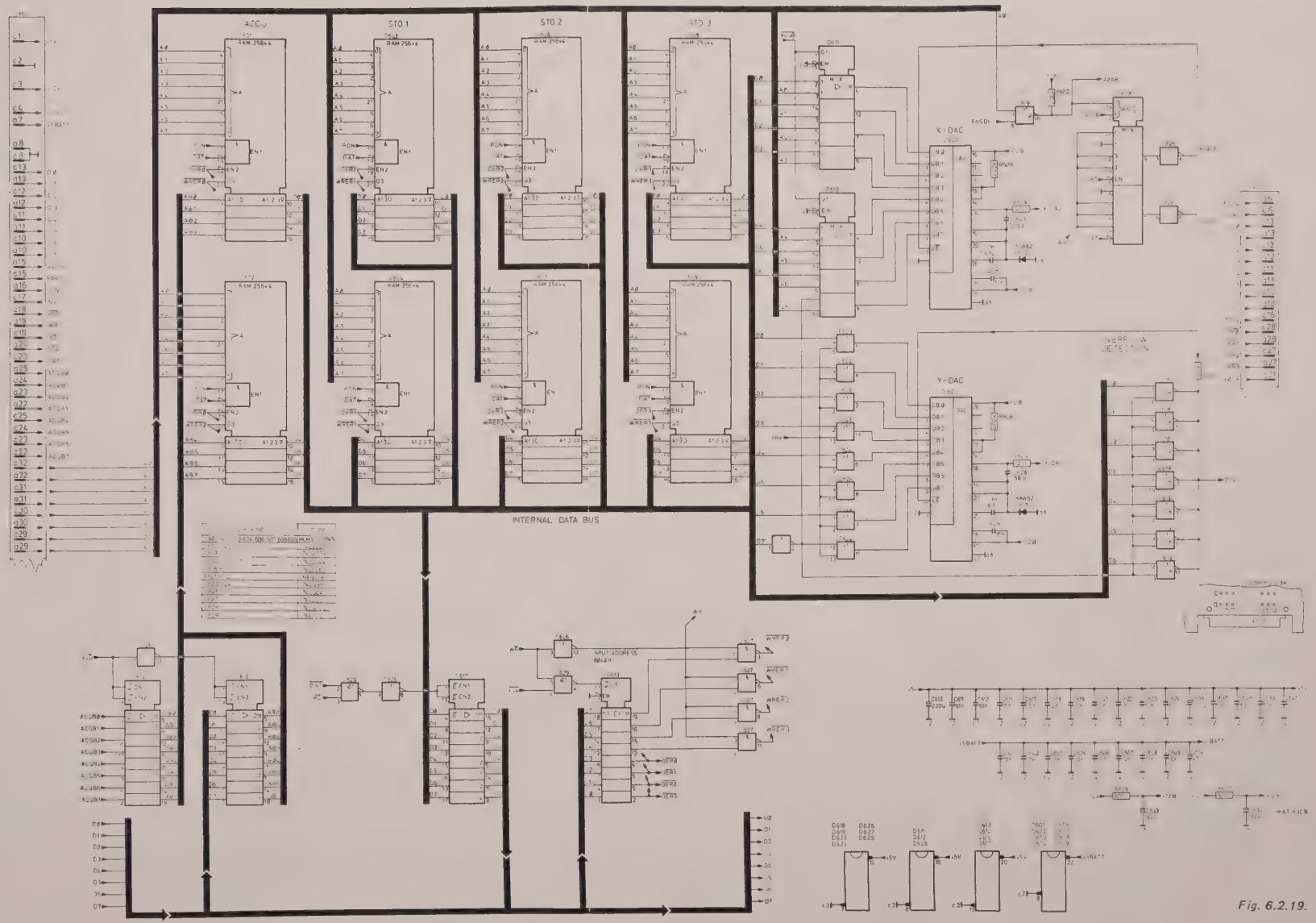


Fig. 6.2.19.

6.2.7. Buffer unit A7

6.2.7.1. General

The buffer unit consists of a 9-bit x 256 digital shift register for data storage and a digital-to-analog converter DAC M-1, which re-converts the digital output signals from the ADC for the correction of subsequent analog signals.

Analog information from the acquisition section of the oscilloscope is converted into a 9-bit digital value ADCBØ ... ADCB8 on the conversion unit. After conversion and final correction, these signal bits are shifted into the 9-bit x 256 digital shift register D701 ... D711 on this buffer unit, for storage.
The contents of this shift register are only shifted under the control of a clock signal CLKSH, generated in D718, D719.

$$CLKSH = \overline{(\overline{INS}.NDR) + (SOD.WR)}$$

Shifting can be interrupted therefore by blocking signal CLKSH.

The nine shift register output signals will only be applied to the ACQB bus in the P^{2}CCD-mode (signal P = logic 1) for correction purposes or if signal NDR = logic 1 (new data is available).
Data is applied to the ACQB bus via the 3-state non-inverting buffers D716 and D717.

6.2.7.2. Data routeing and correction in P^{2}CCD mode

For details of this, refer to the Conversion Unit A8 description.

6.2.7.3. Data routeing and correction in DRS-mode

In the DRS-mode (Direct, Roll and Sample), inaccuracies of the Track/Hold circuit and the ADC circuit are corrected before the information is stored in the shift register.
The circuit is operative for dual-channel mode working, i.e. with both channel A and channel B switched on. This mode is arranged to function automatically even if only one channel is selected.

Principle of operation

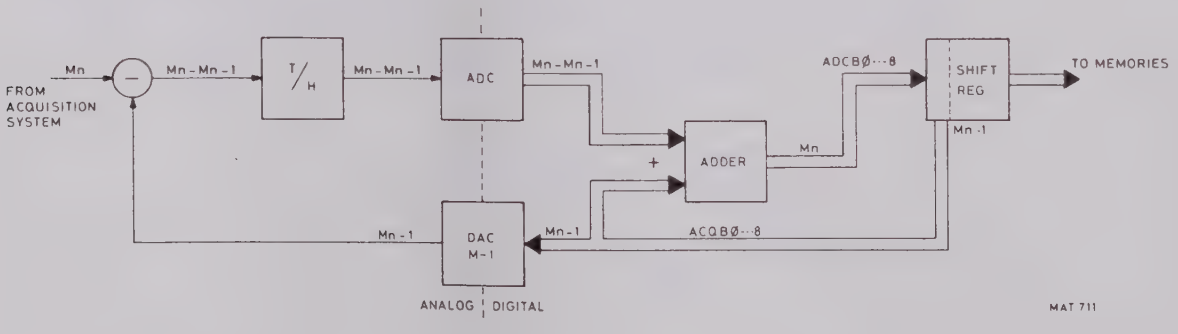


Fig. 6.2.20

To reduce errors in conversion, analog samples for digitising are compared with preceding samples, these being subtracted so that only small increments are converted to digital values in the ADC. After conversion, the digital equivalent of the original analog signal is produced by adding the differential signal from the ADC to the digital value of the preceding sample.

Referring to the block diagram, M_n is the new sample of the input signal from the acquisition system; M_{n-1} is the preceding sample, derived from the shift register and re-converted by DAC M-1 to analog form. At the input to the Track and Hold circuit, M_{n-1} is subtracted from M_n to produce a differential analog voltage, which is then converted to digital form in the ADC and added to the preceding digital value M_{n-1}.

$$\text{i.e. } (M_n - M_{n-1}) + M_{n-1} = M_n$$

After this procedure, the adder output value M_n will be shifted into a shift register as a new and corrected value. This system of digital adding is also used, in a different way, in the P^2CCD-mode as described in the Conversion Unit A8.

Detailed description

This digital adding technique is now described in greater detail with reference to the various circuit elements. The analog value of the preceding signal sample M_{n-1} is subtracted from the new sample M_n in the vertical amplifier stage. This results in a differential analog voltage $M_n - M_{n-1}$, which is converted to digital signals ADCBØ ... ADCB8 and applied to the adder circuit on unit A8 together with the preceding sample M_{n-1} in digital form.

After adding overflow detection and marking, the sum signal M_n is applied as ADCBØ ... ADCB8 to the shift register on the buffer unit A7. With this new signal value stored in the shift register, the circuit continues with the next.

The corrected sample value M_n on the ADCB lines from the conversion unit A8 to the shift register is also applied to the 4-bit latches D712 and stored under the control of signal CØ. The output signals from the latches are applied to the digital-to-analog converter DAC (M-1) D714.

In the P-mode, the DAC (M-1) circuit is switched off by the P signal on the $\overline{LE}$ input pin 10.
However, in the DRS-mode the DAC (M-1) circuit is switched on.
The most-significant bit of the 8-bit 2's complement information offered to the DAC (M-1) is inverted by D719 (4,5) to translate the data into 8-bit straight binary notation.
Conversion by DAC (M-1) results in the analog value of the preceding digital sample M_{n-1} and this value is fed back to the vertical amplifier stage for subtraction from the new signal sample M_n.

In the amplifier stage, analog subtraction will result in a new differential voltage as previously described. This differential voltage $M_n - M_{n-1}$ is then converted to digital in the ADC and added to the old digital value M_{n-1}.
The old digital value that was stored in the two 4-bit latches D712 is in the meantime shifted to the next two 4-bit latches D713 by control signal C4 and fed to the adder circuit. Here, the 8-bit 2's complement notation is converted into a 9-bit ACQBØ ... ACQB8 digital form by copying the last bit.
Data from one signal source only may be fed to the ACQB bus by more than one buffer simultaneously. This is made possible by signals P and NDR via NOR-gate D718 (4,5,6) and inverter D719 (2,3).
Each time an NDR pulse is generated, the total shift register contents will be copied into the ACCU memory.
Precise timing diagrams are given in the ACL Unit A9 description.

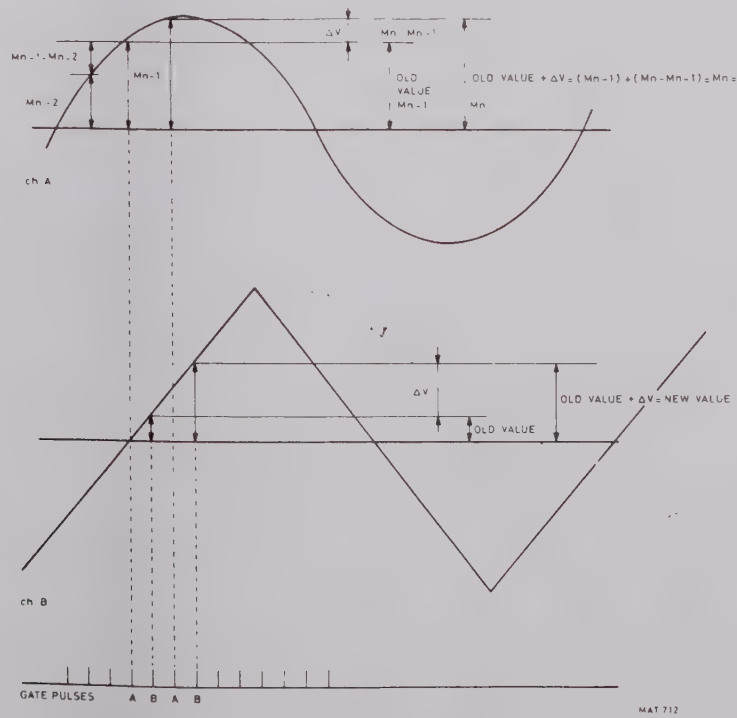


Fig. 6.2.21.

INCOMING SIGNALS	OUTGOING SIGNALS	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	ACQB0 ... 8	A7	A6–8	Acquisition output bits 0 ... 8
ADCB0 ... 8		A8		ADC bits
C0		A9		Control 0 signal from ACL unit
C4		A9		Control 4 signal from ACL unit
	CLKSH	A7		Clock pulse for shift register
	DAC M-1	A7	A21	DAC M-1 output signal
INS		A9		Shift command for shift register
NDR		A9	A4	New data ready
P		A12	A7–8–9–10	P-mode signal
$\overline{\text{SOD}}$		A4		Microprocessor serial output data
	SOD	A7	A8	Microprocessor serial output data
$\overline{\text{WR}}$		A4		Signal write from microprocessor
+5 V		A15		
+12 V		A15		
–12 V		A15		
		A15		

BUFFER UNIT A7

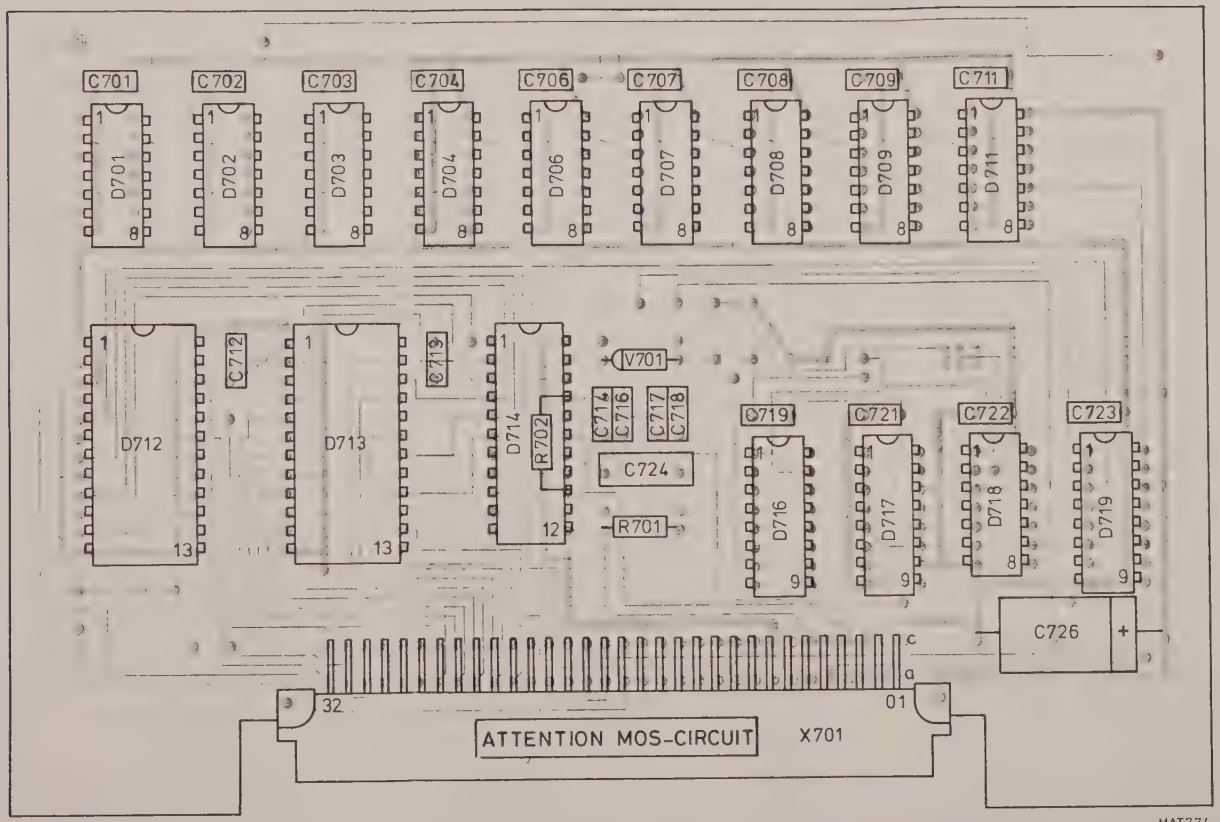


Fig. 6.2.22.

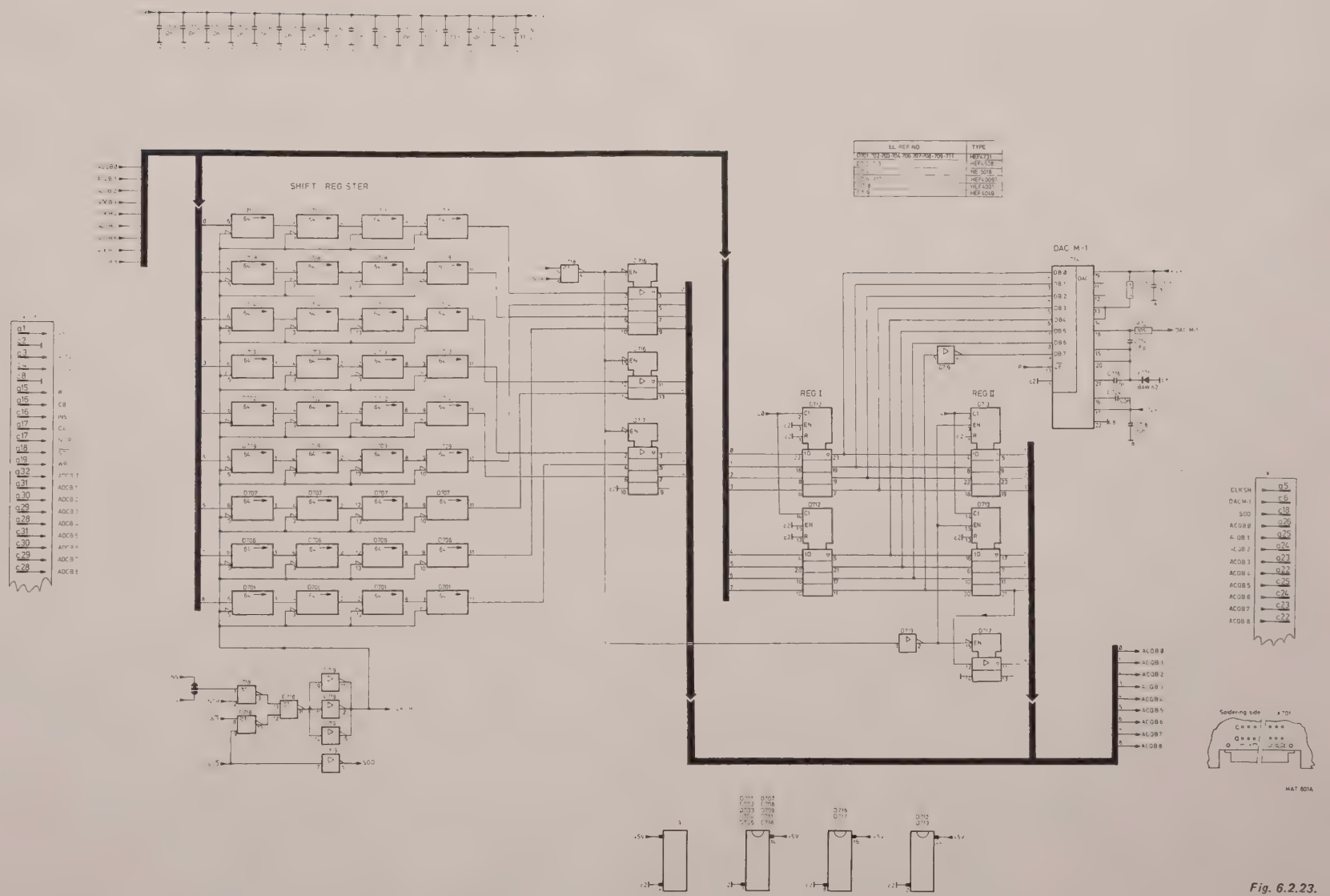


Fig. 6.2.23.

6.2.8. Conversion unit A8

The conversion unit basically consists of an ADC for converting the input signals into digital form for storing in the shift register on the buffer unit A7, a circuit for signal zero correction, and an overflow detection and marking circuit.

These functions are performed by the following circuit blocks:

- a sample and hold circuit for analog inputs, D822
- analog-to-digital converter (ADC) D821
- AND-gates D801, D813 for controlling inputs to the adder circuit
- exclusive-OR gates D802, D814, D809 for inverting signal to adder for subtraction during correction
- adder circuit D803, D816, D804
- multiplexers D806, D807, D817, D818 on adder outputs for overflow detection, marking, etc.
- result registers D819, D811 for storing multiplexer output signals.

6.2.8.1. Sample and Hold circuit

Analog output signal VOUT from the CCD logic unit (A10), which represents the A and/or B channel input signals in one of the selected modes, is applied to input 3 of the sample and hold circuit D822. This circuit is controlled by the TRACK signal:

TRACK = logic 1 — the circuit only tracks the input signal

TRACK = logic 0 — (= HOLD) the circuit holds the input level that was present at the negative-going edge of the TRACK signal

The output signal of this sample and hold circuit D822 provides an input to the ADC that lies between +5 V and –5 V.

6.2.8.2. Analog-to-digital converter (ADC)

The analog input level from the sample and hold circuit is converted into a digital 9-bit number in the ADC circuit D823.
Conversion is controlled by the clock pulses CLADC. (Nine clock pulses are used to convert to this 9-bit number). As the ADC is a 10-bit type, the least-significant bit being ignored. These clock pulses are only generated by the ACL unit A9 during the period when the CONV signal (conversion) is at logic 1.

The ADC output signal CONV reverts to logic 0 at the end of the conversion period, thus indicating that conversion is complete and that the results can be fed to the ADCBØ ... ADCB8 bus via the tri-state non-inverting buffers D811, D812.

The 9-bit digital output of the ADC is straight binary coded and is converted to 2's complement notation in exclusive-OR gate D809 (11,12,13) by inverting the most-significant (9th) bit, as shown in the following table.

	STRAIGHT BINARY (9-bit)			2's COMPLEMENT (9-bit)		
	Decimal			Decimal		
–5 V	+0	0	0 0 0 0 0 0 0 0	–256	1	0 0 0 0 0 0 0 0
		0	0 0 0 0 0 0 0 1	–255	1	0 0 0 0 0 0 0 1
		0	1 0 0 0 0 0 0 0	–128	1	1 0 0 0 0 0 0 0
		0	1 1 1 1 1 1 1 1	–1	1	1 1 1 1 1 1 1 1
		1	0 0 0 0 0 0 0 0	+0	0	0 0 0 0 0 0 0 0
		1	0 1 1 1 1 1 1 1	+127	0	0 1 1 1 1 1 1 1
+5 V	+511	1	1 1 1 1 1 1 1 1	+255	0	1 1 1 1 1 1 1 1

INVERSION OF THE 9th BIT

The 2's complement equivalent value is fed to the ADCB bus-lines by the tri-state non-inverting buffers D811, D812 under the control of signal C1. With C1 at logic 1, the buffers are in 3-state mode.

Signal input C1 is a control line which, together with signal C2 prevents simultaneous input of data to the bus-lines by more than one buffer.

6.2.8.3. Correction circuits

As the correction circuits operate in conjunction with other circuits that are not part of the conversion unit A8, the data routeing and the principles of correction in the P^2CCD-mode are first discussed.

Data routeing and correction in the P^2CCD-mode

Due to internal P^2CCD faults and differences between the frequencies f_{in} and f_{out}, an incorrect zero level of the P^2CCD output signal is possible as shown in the following graph.

Fig. 6.2.24.

P^2 CCD output signal with shifting zero level

Under these conditions, the total faulty contents of the P^2CCD are converted from analog form to digital in 256 steps and after each conversion the data is put on the ADCBØ ... ADCB8 bus and directly shifted into the 9-bit shift register on buffer unit A7. After 256 steps, the total P^2CCD contents are stored here, and the register is then blocked.

In order to correct the zero level, the P^2CCD input is switched to zero and 256 samples of this zero signal are shifted into the P^2CCD at the same frequency f_{in} as for the normal input signal.

By reading the P^2CCD contents again, with the same frequency f_{out} (78 kHz) as for the faulty input signal, an incorrect zero level having the same errors as described above will appear on the P^2CCD output as shown below.

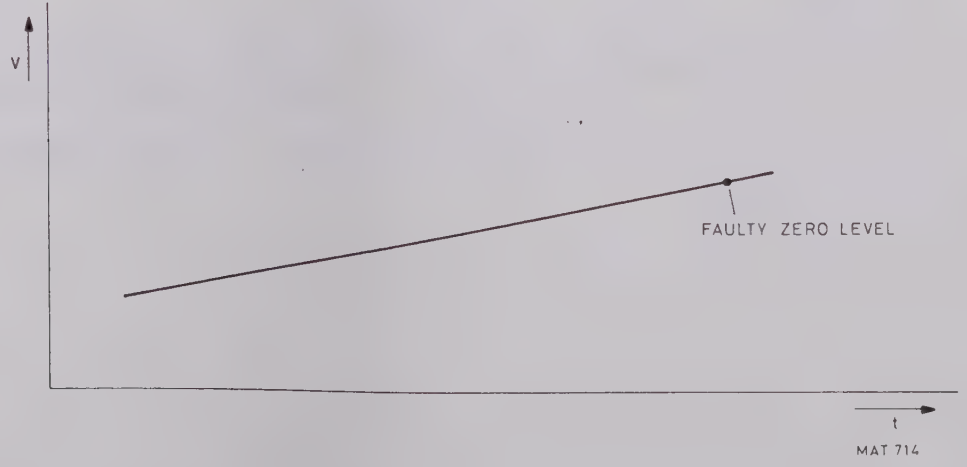


Fig. 6.2.25.

This incorrect zero level is then digitally subtracted (in 256 steps) from the faulty input signal, which was already stored in the shift register.
The corrected result is then re-stored in the shift register.

Correction circuit description

Considering the correction circuits in more detail, the correction cycle is started when the P2CCD is completely filled with zero samples. This is done in 256 steps, in which for every step, one sample of faulty input information from the shift register, and one converted zero sample from the P2CCD are applied to an adder circuit on this conversion unit (A8), consisting of the integrated circuits D803, D816 and D804.

The procedure is as follows:

- The shift register contents are placed byte after byte on the ACQBØ ... 8 bus via a buffer and directly applied to the inputs of the adder circuits.
- The samples of zero information from the P2CCD are placed on the ADCBØ ... 8 bus, sample after sample in the same way as described for the uncorrected signal information. However, in this case it is not shifted into the shift register but is transferred via AND-gates D801, D813 and exclusive-OR gates D802, D814 and D809 (4,5,6) to the adder circuit. For correct overflow detection and marking, bit 9 is copied and applied to the adder as bit 10.

  (During the copying of the shift register contents into the ACCU memory in ROLL-mode, one side of the adder input is blocked via AND-gates D801, D813 by the $\overline{\text{NDR}}$ signal to permit recirculation of the shift-register contents.)

  The exclusive-OR circuits serve to invert the zero information so that it can be subtracted from the signal information. The subtraction process is performed by inverting the zero information and adding it, together with a forced carry, to the signal information from the shift register.
  The forced carry is obtained by signal P on input 9 of adder circuit D803.

At the output of the adder, the corrected signal samples appear one by one and are transferred to the overflow detecting and marking circuits (multiplexers D806, D807, D817, D818).
The ACCU memory, and thus the c.r.t. display, is 8-bit wide; therefore the corrected adder output signals, which can be 10-bit wide, are checked for overflow. Consequently, if overflow occurs, this condition will be indicated and overflow marking is necessary.

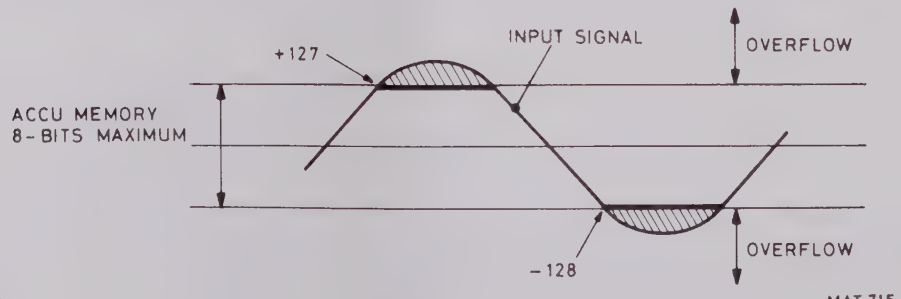


Fig. 6.2.26.

Marking is carried out by changing the signal value during overflow in one of the digital values +127 or −128, via the multiplexers D806, D807, D817, D818.

These multiplexers are controlled by the adder output bits ADOB7, ADOB8, ADOB9, which give information about overflow.

ADOB9	ADOB8	ADOB7	MULTIPLEXER OUTPUT
0	0	0	ADDER OUTPUT
0	0	1	+127
0	1	0	+127
0	1	1	NON-EXISTING
1	0	0	COMBINATIONS
1	0	1	−128
1	1	0	−128
1	1	1	ADDER OUTPUT

In case of an overflow, signal ADOB9 indicates whether it is an overflow or an underflow. ADOB8 and ADOB7 together indicate whether there is an overflow condition.
After marking, the multiplexer output signals are stored in the result register D819 under the control of C3. These output signals are applied to the bus ADCBØ ... 8 via D819 and D811 when signal C2 is logic 0.
C2 = 1 indicates that the buffer outputs are in tri-state.
At the same time, the last bit is copied to re-establish a correct 9-bit 2's complement notation.

The data placed on the bus in this way are the corrected samples and are shifted again into the shift register. After 256 correction steps the shift register contains the complete corrected signal.

Signal NDR (new data ready) now reverts to logic 1 and the shift register contents are copied into the ACCU memory under the control of the microprocessor and its software.

The contents of the shift register are copied into the ACCU memory including the overflow markings +127 or −128. The overflow markings are detected by hardware when the contents of the ACCU are required to be displayed on the c.r.t. screen. This results then in a flashing trace on the c.r.t. screen to indicate this overflow. The same is possible if the ACCU-memory contents are saved in one of the memories STO1 - STO2 or STO3.

Signal $\overline{\text{CLR}}$ enables zeros to be placed on the bus to reset the shift register contents in case of ACCU-memory clearing.

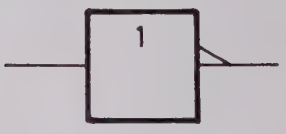
Data routeing and correction in DRS mode

Refer to description of buffer unit A7.

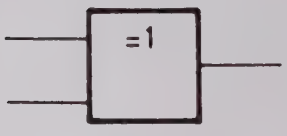
Note: For timing diagrams and explanation of timing refer to the description of the ACL unit A9.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
ACQBØ ... ACQB8		A7		Acquisition output bits Ø ... 8
	ADCBØ ... 8	A8	A7	ADC output signals bit Ø ... bit 8
C1		A9		Control 1 signal from ACL unit
C2		A9		Control 2 signal from ACL unit
C3		A9		Control 3 signal from ACL unit
CLADC		A9		Clock signal for ADC
$\overline{\text{CLR}}$		A4		Clear signal for shift register
	CONV	A8	A9	Conversion
$\overline{\text{NDR}}$		A9		New data ready
P		A12		P2CCD-mode
SOD		A7		Microprocessor serial output data
TRACK		A9		Track command from ACL unit
VOUT		A10		CCD logic unit analog output signal
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor

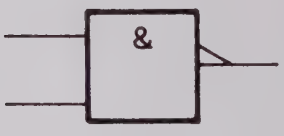
BASIC SYMBOLS



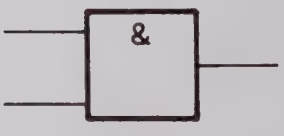
Inverter



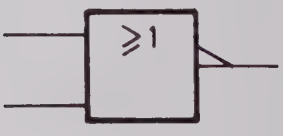
Exclusive — OR



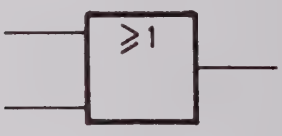
NAND (inverting AND)



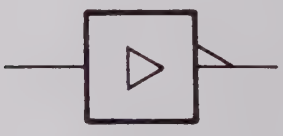
AND



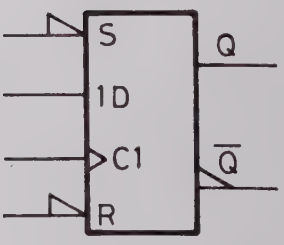
NOR (inverting OR)



OR



Inverting emitter — follower



D — type flip flop

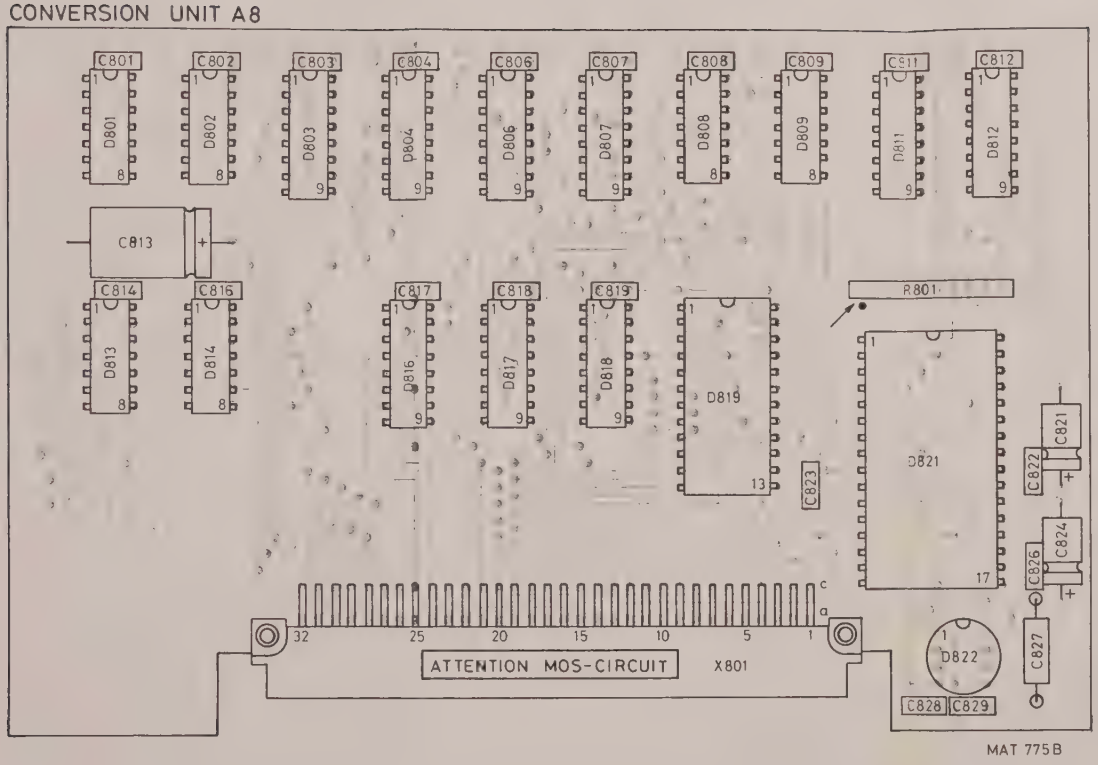

CONVERSION UNIT A8
C801
C802
C803
C804
C806
C807
C808
C809
C811
C812
D801
D802
D803
D804
D806
D807
D808
D809
D811
D812
C813
C814
C816
C817
C818
C819
D813
D814
D816
D817
D818
D819
R801
D821
C821
C822
C823
C824
C826
C827
D822
C828
C829
32
25
20
15
10
5
1
ATTENTION MOS-CIRCUIT
X801
MAT 775B

Fig. 6.2.27.

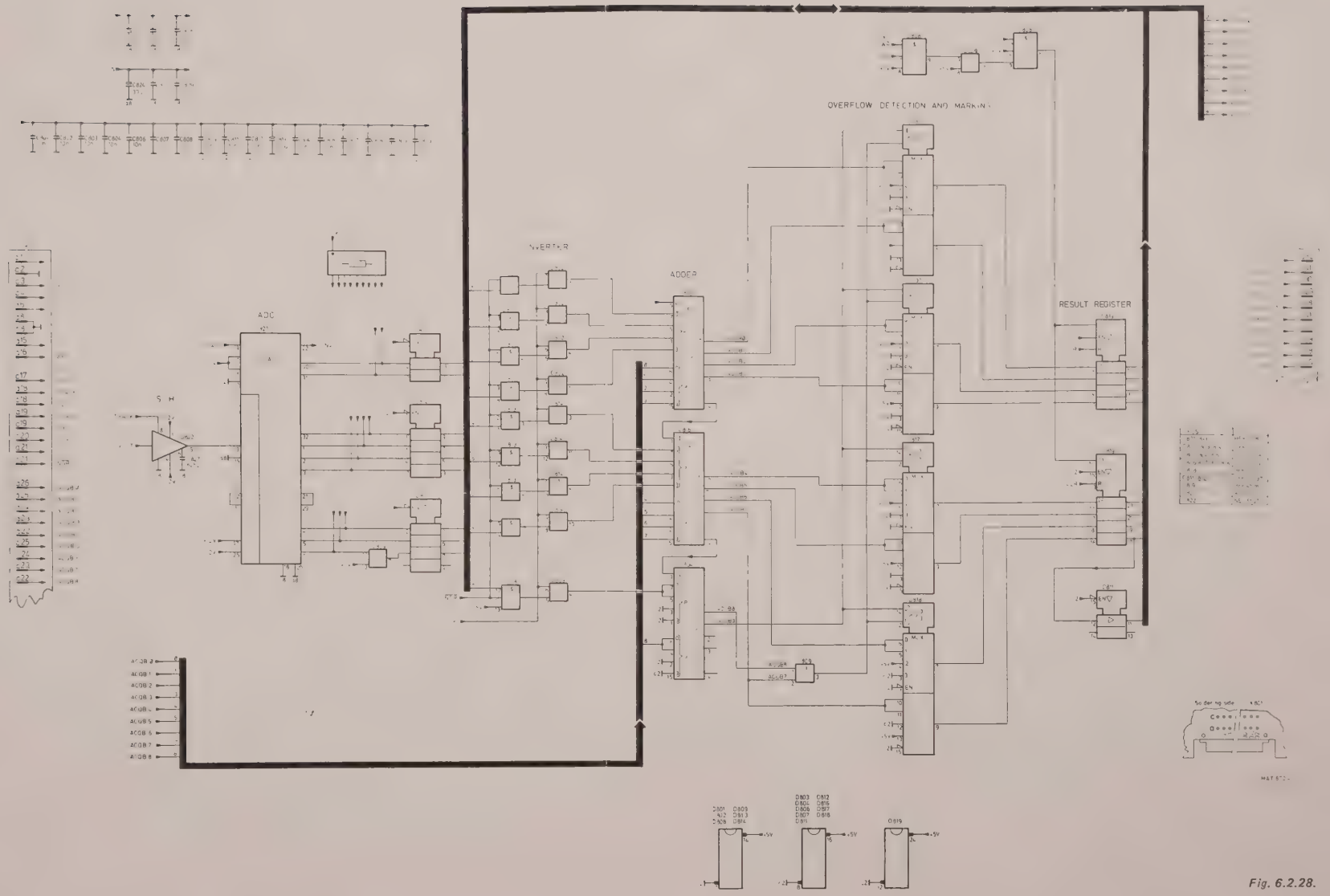

OVERFLOW DETECTION AND MARKING
INVERTER
ADDER
RESULT REGISTER
ADC
S H

Fig. 6.2.28.

6.2.9. Acquisition control logic unit A9

6.2.9.1. General

Before discussing the timing functions in the various operating modes, the general circuit functions of the Acquisition Control Logic unit are first outlined. The ACL unit contains the timing circuits that generate the signals required to control the conversion unit (A8) and the buffer unit (A7).

A Hold and Convert pulse HOCON starts each analog-to-digital conversion of an input signal sample. In the P-mode, this is signal HOCON P from the CCD logic unit A10; in the Direct, Roll and Sampling modes, this is HOCON DRS from the trigger unit A22.
Depending on the mode selected, one of these hold and convert signal lines is applied to the clock input of D-type flip-flop D909 via multiplexer D911, pin 7. This multiplexer is controlled by the signals P and R, to give the following:

SIGNALS R	SIGNALS P	D911 output pin 7
0	0	HOCON DRS
0	1	HOCON P
1	0	HOCON DRS
1	1	(unavailable input signal combination)

Flip-flop D909 is switched by the HOCON pulse, resulting in the TRACK signal going to logic 0, which brings the Track and Hold circuit on the conversion unit to the HOLD state.
Analog-to-digital conversion is now started and controlled by the nine clock pulses CLADC (pin 11 of NAND-gate D906), which are derived from a 1,25 MHz clock signal. During conversion in the ADC, a signal CONV is at logic 1. After conversion, this signal goes to logic 0, indicating that conversion is finished. Output pin 6 of flip-flop D909 is now switched to 0 by the $\overline{\text{CONV}}$ signal and this zero resets the other two flip-flops in the circuit (RESET inputs D908-12, D909-13). In this way, the CONV signal blocks the CLADC pulses again and switches the TRACK signal. The track and hold circuit now returns to tracking the input signal.

The CHOP output of chopper flip-flop D908 is switched to its opposite state at the end of each conversion by signal $\overline{\text{CONV}}$ on its clock input. Only in the P-mode, where the CHOP signal is not required, is the chopper flip-flop set permanently to its '1'-state, i.e. signal CHOP is logic 1. This is achieved by a zero level on the direct set input of the flip-flop.

During each conversion, a CØ pulse on D906-8 is fed from the CONV signal to control the first buffer stage (D712 on unit A7) after the adder circuit (on unit A8). This is the buffer stage that sends its data to the digital-to-analog converter DAC (M-1).

At the completion of each ADC conversion, counter D928, which has been preset to the value 15, starts counting the 1,25 MHz pulses on its clock input.
The start of counting is initiated by the output signal of flip-flop D927, which is set to logic 1 by the positive-going edge of the $\overline{\text{CONV}}$ signal.

	OD	OC	OB	OA
15 →	1	1	1	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1

The first counting pulse results in counter-state 0. Output signals OA, OB, OC and OD are applied to a BCD/1 : 10 decoder, D923.
Control pulses C3 and C4 are derived directly from decoder outputs 3 and 4 respectively. The C3 pulses are only present whenever there is no new data ready, i.e. if $\overline{NDR}$ = logic 1.
After state 7 of the counter, a logic 0 on output pin 9 of the decoder is fed back to the direct reset input of flip-flop D927 to switch it to its zero state. Thus the count pulses for the counter are blocked and it is again preset by the value 15. From the same decoder output signal a COUNT pulse is given via flip-flop D913, which is switched as a normal inverter. One COUNT signal is generated for each ADC conversion and so provides a means of counting the number of conversions.

Control pulses C1, C2 (C1 inverted) and INSP are generated by multiplexer D921 controlled by the NDR and PN signals.

CONTROL SIGNALS		OUTPUT SIGNALS	
NDR	PN	C1	INSP
0	0	OC	INSR
0	1	0 V	$\overline{C3}$
1	0	+5 V	+5 V
1	1	+5 V	+5 V

Signals C1 and INSP are permanently at logic 1 during NDR. Therefore, during copying the contents of the shift register into the ACCU memory, the buffer following the ADC circuit will be set in its tri-state, i.e. no ADC output data can be sent either to the adder or to the shift register circuit.

Signal C1 will be at logic 1 when uncorrected signal information has to be shifted into the shift register in the P-mode (PN at logic 1). This allows the information to be shifted directly into the register. The shift command INSP is in this situation derived from signal $\overline{C3}$. In the DRS modes and during zero correction in the P-mode, C1 and also C2 signals are derived from counter output OC. These signals control the ADC output buffer and the adder output result register (D819 on unit A8) so that only one of the two can output data on to the ADCBØ ... 8 bus at any given time.
In the DRS modes, and during zero correction in the P-mode, the INSP signal is derived from decoder output signal INSR. Therefore, INSP is generated after the correction result is put in the result register and the register output data is fed to the ADCBØ ... 8 bus.

6.2.9.2. Timing in P-mode

Flip-flop D913 is set to logic 1 by a trigger pulse DELTRG in normal trigger mode and by $\overline{AUTRI}$ in the AUTO mode, both signals being generated by the delayed trigger unit (A13).
After receiving a trigger signal, the NULIN signal goes to logic 1. This signal is applied to the vertical amplifier unit A21 to block the amplifier channels so that a zero level is offered to the P^2CCD inputs.
A signal $\overline{FOE}$ (frequency output enable) also goes to logic 0 (assuming that pin 10 of D914 is at logic 1) to indicate to the CCD logic unit that the P^2CCD contents can be read with a clock signal of 78 kHz approx. This will result in HOCON P pulses to start ADC conversions.

The COUNT signals generated at each conversion are counted by the 10-bit acquisition control logic counter consisting of two flip-flops D924 and two 4-bit counters D918 and D917.
This counter, which was in its reset state in the preceding P-mode cycle, is now enabled for counting. Signal NUL IN switches, via multiplexer D916, the flip-flop D902 so that the counter is no longer held in its reset state and is ready to receive count pulses. Signal $\overline{FOE}$ sets the multiplexer D926 so that the COUNT pulses on input 12 appear at output 9. These COUNT pulses are applied to the counter and after 256 have been counted the entire P^2CCD contents are read, digitised and shifted into the shift register. Counter state 256 is indicated by a logic 1 on pin 12 of D917. This signal switches $\overline{FOE}$ to logic 1 via inverter D919 and NAND-gate D914 to stop the P^2CCD read cycle.

A cycle now starts in which the P²CCD is completely filled with zero information, using the same frequency for shifting as that for reading in the input signal information.
Signal $\overline{FOE}$ now switches multiplexer D926 to the state where the 50 kHz signal on pin 13 is coupled to the input of the counter. Counting continues up to 512 and in the meantime, zero information is shifted for about 5 msec into the P²CCD via the NUL IN signal in the vertical amplifier unit (256 x 0,02 msec is approximately 5 msec).
When the counter reaches 512, output 12 of D917 returns to logic 0 and also signal $\overline{FOE}$ = logic 0.
Now a cycle starts in which the zero contents of the P²CCD are read and digitised in 256 steps at a clock frequency of approximately 78 kHz. At every step, one sample of uncorrected information in the shift register is corrected by a zero sample from the P²CCD and the result shifted again into the register. After 256 corrections the total corrected signal is present in the shift register.
At the end of the correction cycle, the state 768 (512+256) of the counter is detected by NAND-gate D914 (11,12,13), which results in a logic 0 on output pin 11.

This signal is fed to output pin 9 of multiplexer D916 and causes flip-flop D902 to switch to its zero state. The output signal on pin 9 of D902 prepares the reset of two synchronous counters with synchronous clear, D918, D917. These can now be reset by a pulse on the clock input, which is derived from a 1,25 MHz clock signal via D926 and D924. The clock signal can pass through multiplexer D926 because of the low level of the output signal on pin 9 of D916, which is applied to input 2 of D926.

After the reset of counters D918 and D917, the output pin 3 of NAND-gate D914 goes to logic 0 via the multiplexer and NAND-gate D914 (11,12,13). This signal resets the two flip-flops D924 of the acquisition control logic counter. The entire counter is now in the reset state and remains in this state until the next NUL IN signal is generated.

At the end of the correction cycle, the positive-going edge of the signal on output 8 of flip-flop D902 will, via multiplexer D901, switch NDR flip-flop D902 to its logic 1 state. Signal NDR is applied to the SID input of the microprocessor on unit A4 to indicate that new data is ready and can be copied by the ACCU memory.

After a certain time, the microprocessor reacts by generating a logic 1 on its SOD output and 256 $\overline{WR}$ pulses followed by a logic 0 on its SOD input. During the SOD signal the shift register contents are copied into the ACCU memory in 256 steps controlled by the $\overline{WR}$ pulses from the microprocessor.

Trigger flip-flop D913 is then brought to its reset state by signal $\overline{CTF}$, which is derived from signal $\overline{NDR}$ via multiplexer D901.
The whole system can react again on incoming trigger pulses at the end of the 'handshake' cycle.

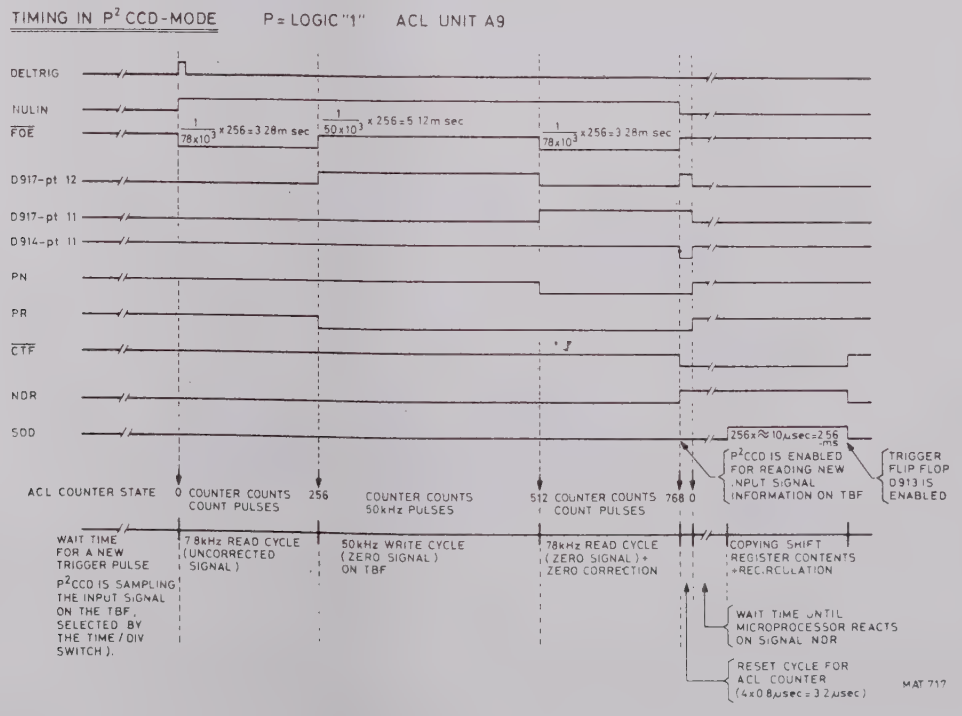


Fig. 6.2.29

Flip-flop NDR is then reset by the positive-going edge of the $\overline{SOD}$ signal via the flip-flop consisting of NAND-gates D903, and signal $\overline{CTF}$ goes to logic 1 so enabling trigger flip-flop D913 again.

The NDR signal will also be generated while the CLEAR button on the front panel is operated.
Signal $\overline{CLR}$ is then at logic 0.

6.2.9.3. Timing in Direct mode

In the Direct mode the flip-flop D913 is switched to logic 1 by a trigger pulse DELTRG in normal trigger mode and by $\overline{AUTRI}$ in the AUTO mode, both signals being generated by the delayed trigger unit (A13).

On receipt of a trigger, flip-flop D913 is switched and applies a logic 1 to the D-input of NDR flip-flop D902 via NAND-gate D903 (1,2,3).
The NDR flip-flop switches to logic 1 at the first COUNT pulse on its clock input (received via multiplexer D901). This commences an NDR cycle to copy the shift register contents into the ACCU memory in the way already described for the P-mode.

The NDR flip-flop is reset by the positive-going edge of the $\overline{SOD}$ signal via the flip-flop comprising NAND circuits D903. Simultaneously, the acquisition control logic counter starts counting 256 COUNT pulses. This start is initiated by the $\overline{NDR}$ signal on the clock input of flip-flop D902, received via multiplexer D916.
At this same start time, a logic 0 on output 8 of flip-flop D902 causes output $\overline{CTF}$ of multiplexer D901 to go to logic 0. This results in a reset of the trigger flip-flop D913.

The acquisition control logic counter counts up to state 256. This state is decoded, resulting in a logic 1 on pin 12 of counter D917, which is applied via inverter D919 (8,9) and multiplexer D916 to flip-flop D902.

The counter is then reset in the way described for the P-mode.

At this moment, it is established that at least 256 new samples of the input signal are stored in the shift register, so the total shift register contents are refreshed (i.e. a type of trigger hold-off).

Resetting the acquisition control logic counter results in signal $\overline{CTF}$ going to logic 1, thus again enabling the trigger flip-flop D913.
This prepares the flip-flop to receive another trigger to start a new D-mode cycle.

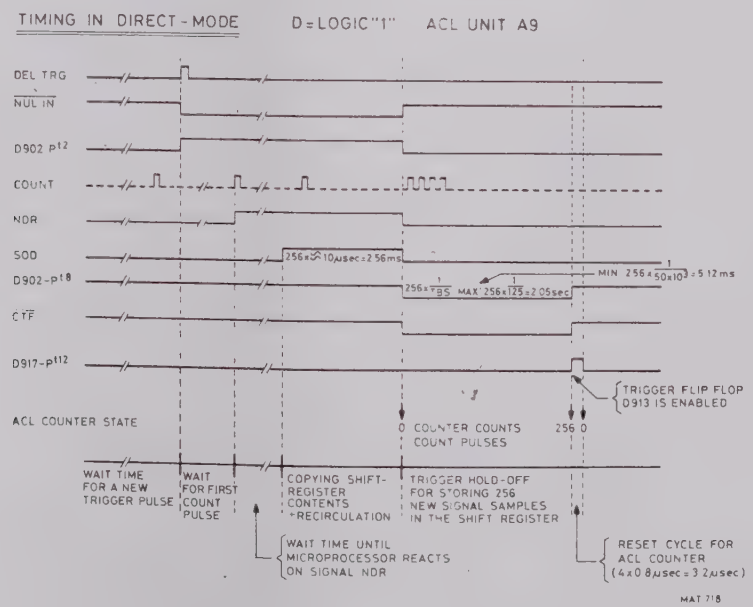


Fig. 6.2.30.

6.2.9.4. Timing in Roll mode

If ROLL-mode is selected and the RUN/STOP pushbutton is pressed once, the ROLL-mode action is started by TBS pulses generated on time-base unit A12 after a start signal from the microprocessor.
HOCON DRS pulses are derived from the TBS pulses on trigger unit A22. Each HOCON DRS pulse applied to the ACL unit A9 starts an analog-to-digital conversion of a new input signal sample.
The ACL unit is set to ROLL-mode by the R control signal.
In the ROLL-mode the D-input of the NDR flip-flop D902 is permanently at logic 1 via NAND-gate D903 (1,2,3).
Each time a new signal sample is stored in the shift register, a COUNT pulse is generated and an NDR cycle started as described for the P-mode.

During this NDR cycle, the entire shift register contents are copied by the ACCU memory and re-circulated.

The microprocessor and its software calculate the number of NDR cycles and after each 256 the ACCU memory contents are copied in one of the memories STO3, STO2, STO1 under software control.
The last 256 samples remain in the ACCU memory. The ROLL-mode is now finished, this being indicated by a flashing RUN lamp on the instrument front panel.

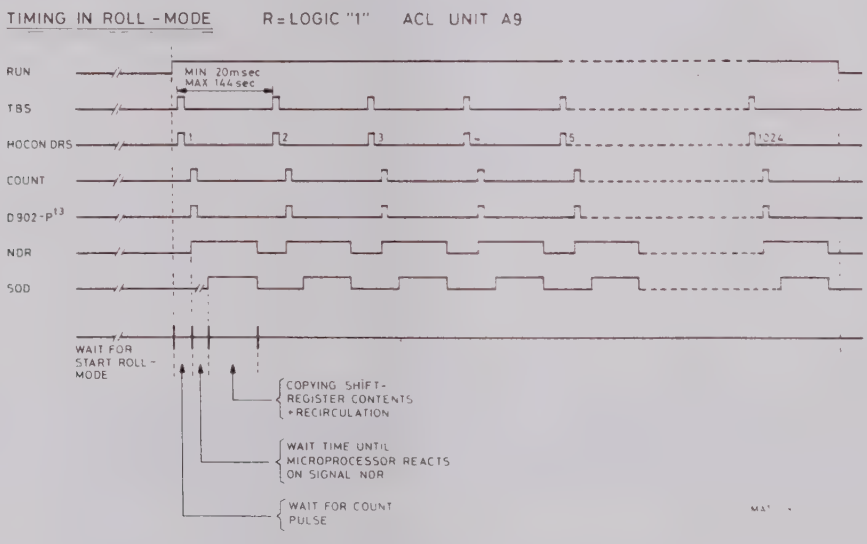


Fig. 6.2.31.

6.2.9.5. Timing in Sampling mode

The control signal S sets the ACL unit in the Sampling mode.

Correct functioning in this mode requires that signals of a repetitive nature are applied to the input channels of the instrument.

Each sampling cycle is started with the staircase counter in the zero position and a pre-determined LEVEL setting.
During one sampling cycle 256 samples of the input signal are stored in the shift register to build a complete signal picture. Each input trigger signal takes one sample of the input signal as now described.

On each trigger signal a fast ramp signal is generated (on unit A22) which is compared with the output of a DAC circuit DACSTAIR, D904. This circuit is coupled to the staircase counter to convert the counter state into the analog signal DACSTAIR.
At the crossover point determined by each comparison of the fast ramp signal and the DACSTAIR signal, an HOCON DRS pulse is generated to start the ADC conversion of the new signal sample.
The time between samples depends on the fast ramp speed which, in turn, is determined by the time-base frequency setting.

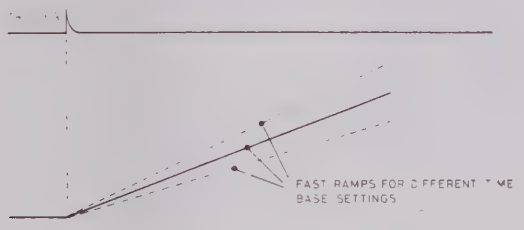


Fig. 6.2.32.

After each conversion, a COUNT pulse is counted by the staircase counter, which causes the DACSTAIR output signal to increase by one step (40 mV).
In this way, the time between the trigger pulses and the generation of the HOCON DRS signal increases so that each new sample is taken one step later.

The shift register is completely filled after 256 samples and its contents can be copied by the ACCU memory. This is initiated by state 256 of the staircase counter. A logic 1 on pin 12 of the counter D917 causes it to reset to zero as already described in the P-mode. The logic 1 level on output 8 of reset flip-flop D902 is fed to the clock input of the NDR flip-flop via multiplexer D901. This starts an NDR cycle and the shift register contents can be copied in the ACCU memory. After this, the staircase counter is again enabled for counting by the positive-going edge of the $\overline{\text{NDR}}$ signal via multiplexer D916 and a new sampling cycle is started.

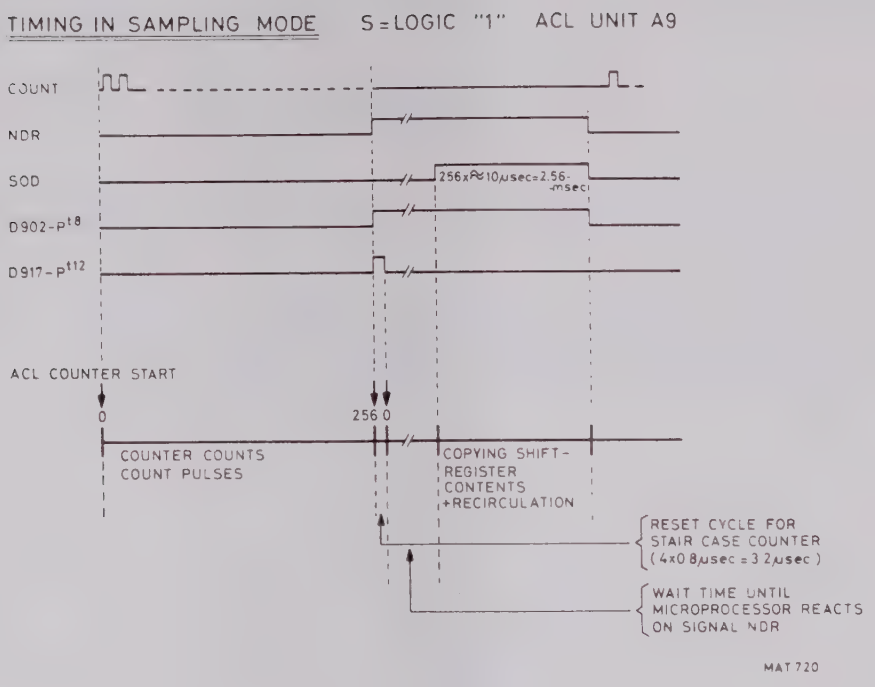


Fig. 6.2.33.

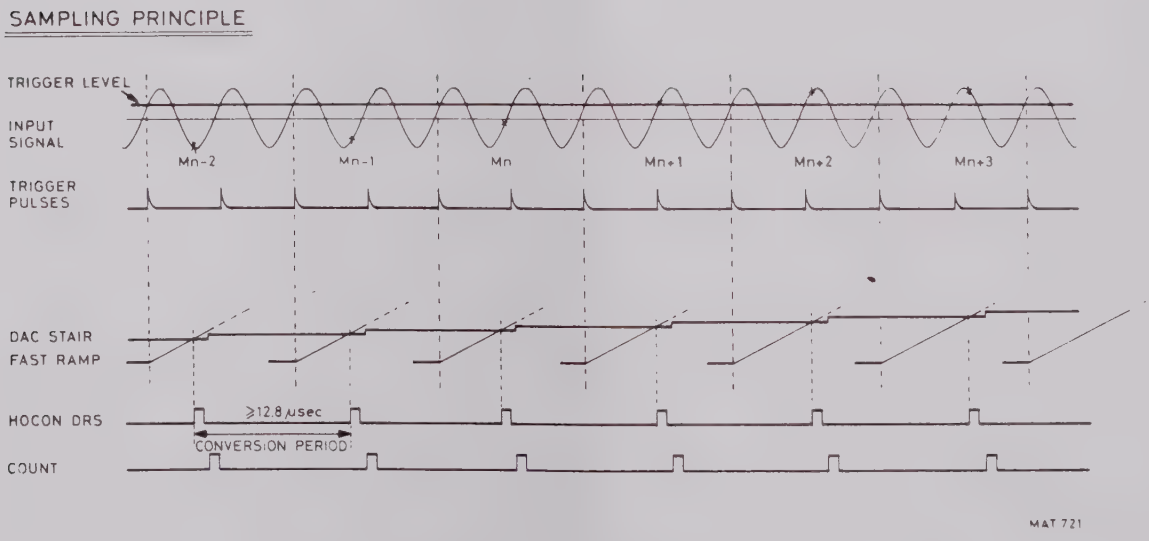


Fig. 6.2.34.

6.2.9.6. *Flip-flop FASA*

The flip-flop FASA stores the information indicating whether the last sample stored in the shift register was from channel A or channel B.

FASA = 1 : channel A was last sample
FASA = 0 : channel B was last sample

In the P-mode, the flip-flop FASA is set to the level of its D-input signal PDRIVE by the leading edge of every INS pulse on its clock input while the PR signal is logic 1 (CHOP is permanently at logic 1 in the P-mode).

In the DRS modes, flip-flop FASA is switched to the level of its D-input signal CHOP by the leading edge of every INS pulse on its clock input (signals PR and PDRIVE are permanently at logic 1 in the DRS modes).

The state of flip-flop FASA cannot be changed while NDR is logic 1, i.e. during the copying of the shift register contents into the ACCU memory. During this cycle the flip-flop state is read by the software.

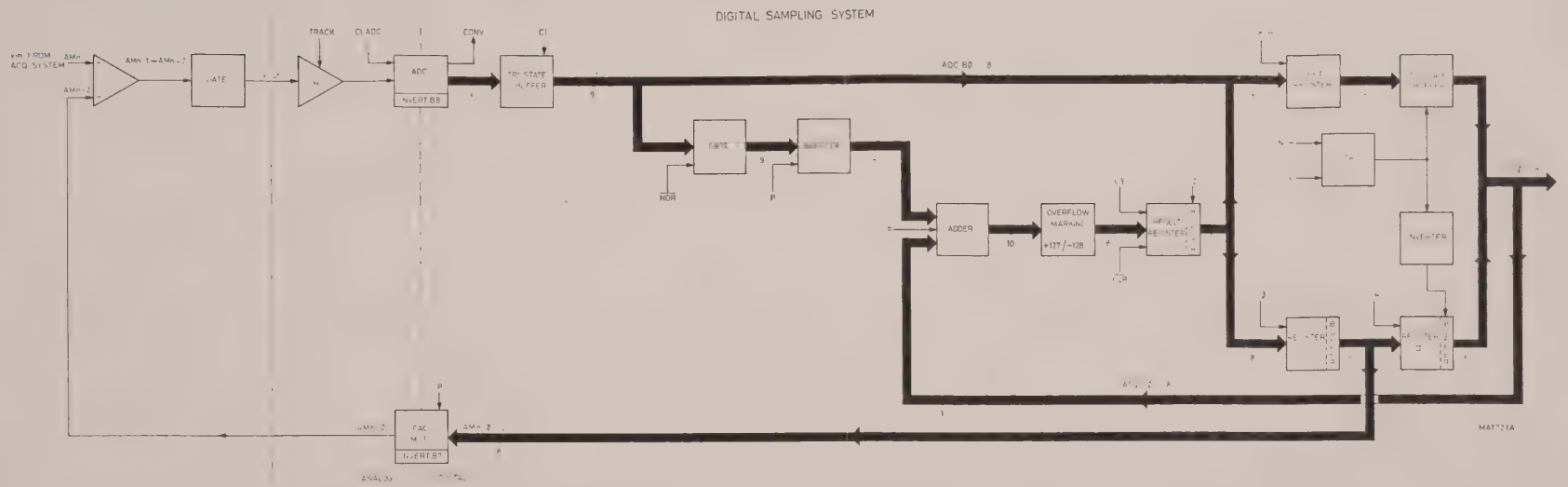


Fig. 6.2.35.

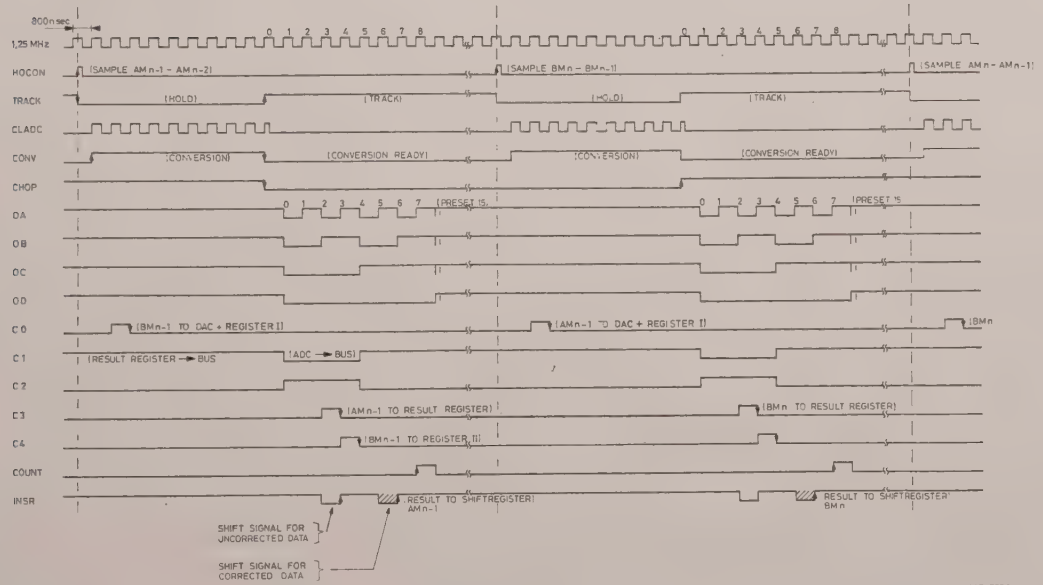
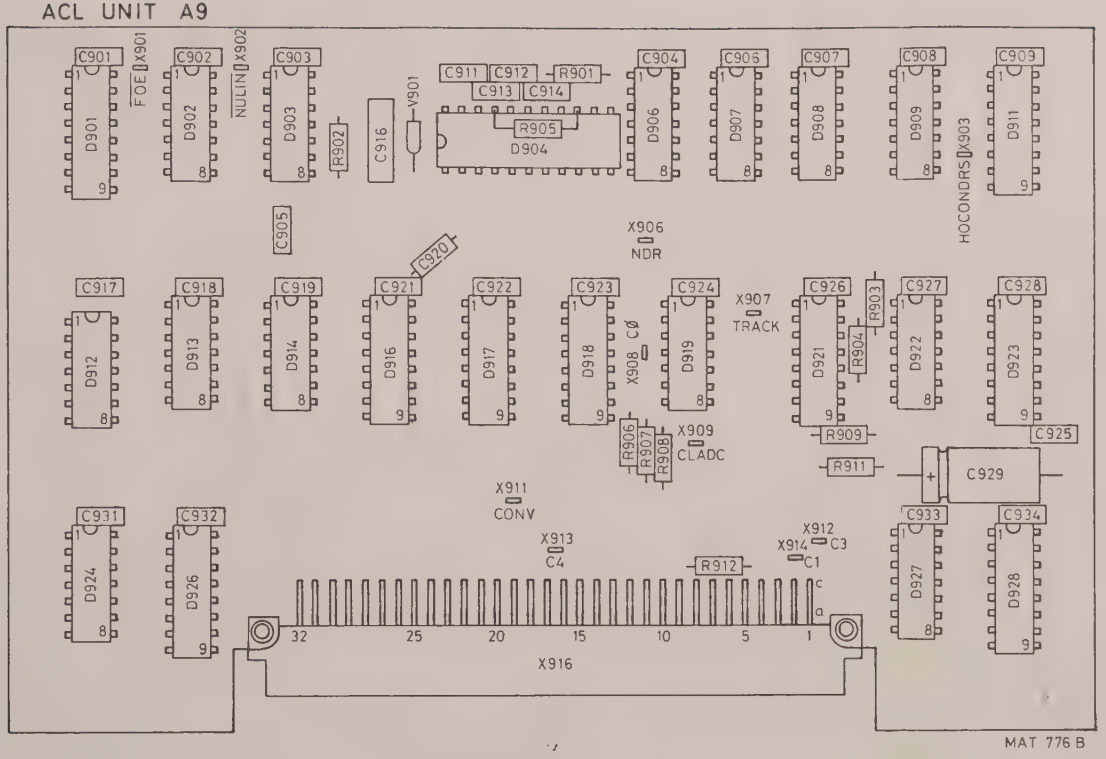


Fig. 6.2.36.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
$\overline{\text{AUTRI}}$		A13		Auto trigger
	CØ	A9	A7	Control Ø signal
	C1	A9	A8	Control 1 signal
	C2	A9	A8	Control 2 signal
	C3	A9	A8	Control 3 signal
	C4	A9	A7	Control 4 signal
	$\overline{\text{CHOP}}$	A9	A21	Chopper signal
	CLADC	A9	A8	Clock signal for ADC
$\overline{\text{CLR}}$		A4		Clear signal for shift register
	CLR	A9	A8	Inverted CLR signal
CONV		A8		Conversion
	$\overline{\text{CTF}}$	A9	A13	Clear signal for trigger flip-flop
D		A12		D-mode signal
	DACSTAIR	A9	A22	Output signal of DAC STAIR
DELTRIG		A13		Delayed trigger signal
	$\overline{\text{EOCØ}}$	A9	A9	Enable output COUNT Ø
$\overline{\text{EOC1}}$		A3		Enable output COUNT 1
	FASA	A9	A202	Output phase flip-flop
	$\overline{\text{FOE}}$	A9	A10	Frequency output enable
HOCON DRS		A22		Hold and convert signal in D-R and S mode
HOCONP		A10		Hold and convert signal in P-mode
	INS	A9	A7	Shift command for shift register
	NDR-$\overline{\text{NDR}}$	A9	A4-7-8	New data ready
	NULIN	A9	A21	Signal to switch vert. ampl. input to zero
P		A12		P-mode signal
PDRIVE		A10		Phase signal in P-mode
	PRES	A9	A10	Enable signal in P-mode.
R		A12		R-mode signal
S		A12		S-mode signal
$\overline{\text{SOD}}$		A4		Microprocessor serial output data
	TRACK	A9	A8-A22	Track command for S/H circuit
50 kHz		A12		50 kHz pulse
1,25 MHz		A12		1,25 MHz pulse
+5 V		A15		
−12 V		A15		
+12 V		A15		
⏚		A15		

TEST POINTS	
X901	$\overline{\text{FOE}}$
X902	NUL IN
X903	HOCONDRS
X904	$\overline{\text{SOD}}$
X906	NDR
X907	TRACK
X908	CØ
X909	CLADC
X911	CONV
X912	C3
X913	C4
X914	C1
X916	EOCØ/EOC1


ACL UNIT A9
C901
C902
C903
C904
C905
C906
C907
C908
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R903
R904
R905
R906
R907
R908
R909
R911
R912
V901
X901
FOE
X902
NULIN
X903
HOCONDRS
X906
NDR
X907
TRACK
X908
CØ
X909
CLADC
X911
CONV
X912
C1
X913
C4
X914
C3
X916
32
25
20
15
10
5
1
c
a
MAT 776 B

Fig. 6.2.37.

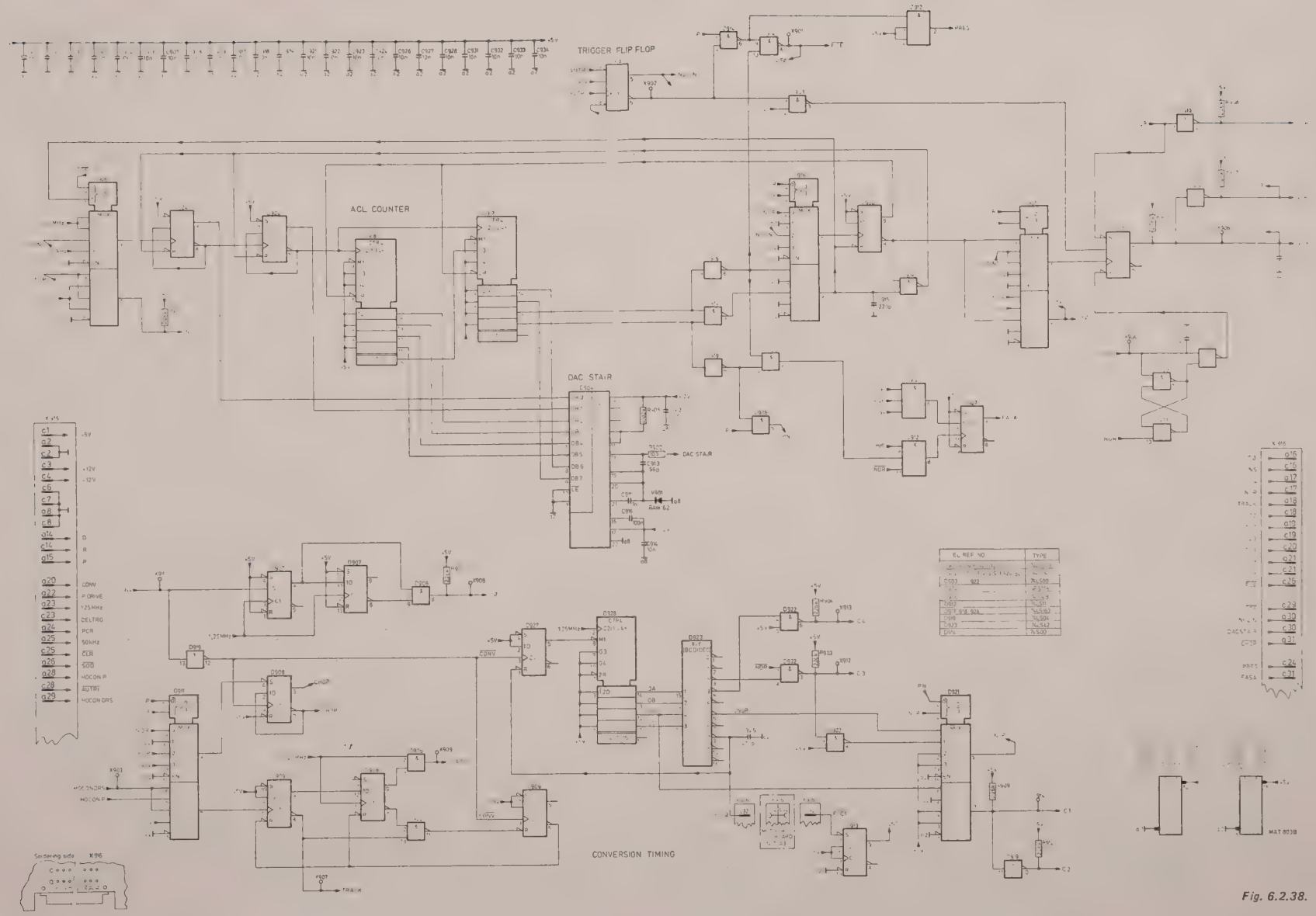

TRIGGER FLIP FLOP
ACL COUNTER
DAC STAIR
CONVERSION TIMING
MAT 8038

Fig. 6.2.38.

6.2.10. CCD Logic unit A10

6.2.10.1. General

The CCD logic unit controls the correct functioning of the P2CCD circuit on unit 11. The control circuits can be considered under the following headings:

- circuits for various supply voltages
- P2CCD external output circuits
- control signals generator
- clock-pulse generator

6.2.10.2. Circuits for various supply voltages

+11,4 V — From the +12 V supply a stabilised +11,4 V is derived by the circuit consisting of D1016 (1,2,3) and transistor V1018.
This +11,4 V supply output can be adjusted by potentiómeter R1080 at the input of D1016.

−11,4 V — A −11,4 V stabilised supply voltage is derived from the −12 V supply by the circuit consisting of D1016 (5,6,7) and transistors V1021 and V1019, The level of the −11,4 V supply is controlled by the stabilised +11,4 V on resistor R1098.

+5B — A +5 V stabilised supply voltage is derived from the +11,4 V at input 1 of D1021.

BIAS — A stabilised bias voltage for the P2CCD input signal circuits is obtained from the stabilised +11,4 V by means of the circuit comprising D1002 (1,2,3) and transistor V1006.
Potentiometer R1002 provides for adjusting this bias voltage and is normally set to +7,5 V approx.

DRAIN — A stabilised drain voltage for the P2CCD output circuit is taken from the stabilised +11,4 V by circuit D1002 (5,6,7) and transistor V1007. Adjustment of this drain voltage is by potentiometer R1008 and is normally set to +22 V approx.

P11IN/P22IN — Two adjustable threshold voltages are available for the P2CCD circuit input sections, which are derived from the stabilised +11,4 V.
These voltages can be adjusted by potentiometers R1026 and R1007 respectively and are normally set to +6 V approx.

SUB — A voltage applied to the substrate input of the P2CCD, adjustable by means of potentiometer R1027 and normally set to +10 V approx.

6.2.10.3. P2CCD external output circuits

Output signals OUT PA and OUT PB (from the two sections of the P2CCD on unit 11) are applied to two output circuits comprising two multiplexers D1018, D1019 and two integrators consisting of operational amplifiers D1009, D1011 and capacitors C1034, C1036.
Both output circuits serve to elliminate output source-follower drift, noise signals and clock-pulse or reset crosstalk signals that would influence the P2CCD output signals.

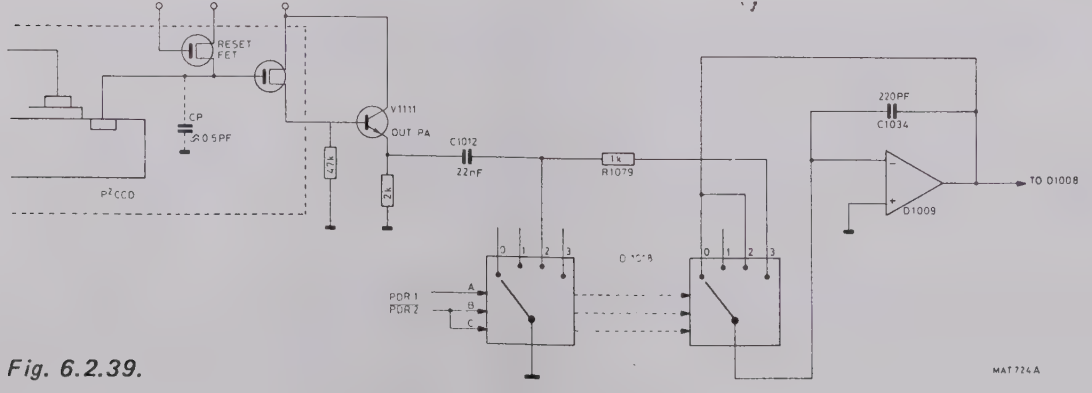


Fig. 6.2.39.

As a result, clean output signals are produced, which are applied via multiplexer D1008 and amplifier stage D1017 to the conversion unit A8 as the V OUT signal.

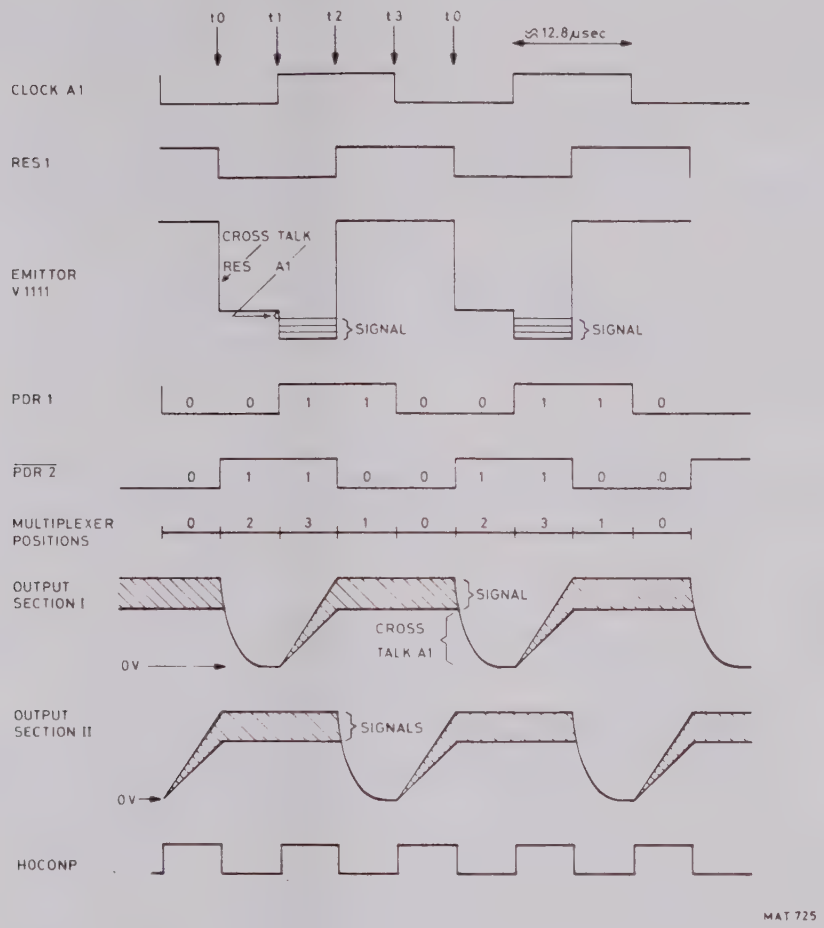


Fig. 6.2.40.

Before time t_o, signal RES1 is at logic 1, which causes the P2CCD reset FET to conduct. The parasitic capacitor C_p of the source-follower gate is then charged to the level of the DRAIN RS1 voltage.

At the moment t_o, signal RES1 switches to logic 0 and the reset FET goes non-conducting.
Due to the crosstalk of signal RES1 present on the source-follower gate, a voltage jump appears on the emitter of transistor V1111.

During the time between t_o, and t_1, the analog multiplexer D1018 is set to position 2 by its control signals PDR1 and $\overline{\text{PDR2}}$, Capacitor C1012 is then charged to the level on the emitter of V1111. At the same time, integrator capacitor C1034 will be discharged to 0 V via position 2 of the multiplexer.

At t_1 (the positive-going edge of the clock-signal A1), a signal sample is fed to the source-follower gate, which results in a change of the voltage across C_p. This voltage across C_p is also influenced by crosstalk from the clock-signal A1. The emitter of transistor V1111 follows the voltage changes across C_p.

During the time between t_1 and t_2, the multiplexer D1018 is set to position 3. The difference between the emitter voltage of V1111 and the voltage across C1012 is now applied across R1079 and is integrated by the circuit D1009 and C1034. As can be seen from the timing diagram, the crosstalk of RES1 is now completely suppressed.

During the time between t_2 and t_3, the analog multiplexer switches to either position 1 or 0, but the multiplexer is not then enabled (signal PDR2 on the enable input G4). The output voltage therefore remains available on pin 6 of D1009.

A similar external output circuit is available for signal OUT PB, resulting in integrated voltages on pin 6 of D1011. Because of the differences in control signals PDR1 and PDR2, the signals are 180° phase-shifted.

The signals that are read into the P²CCD for temporary storage need to be converted into digital information for permanent storage in a digital memory.
For this purpose, the output signals on pins 6 of D1009 and D1011 are applied to a multiplexer, D1008.

This multiplexer switches both P²CCD output signals to one single serial output signal V OUT, when P-mode is selected (signal P at logic 1).
Signal PDR2 is responsible for switching over from output section I to output section II. For the DRS modes the multiplexer D1008 switches the signal DRS to its output V OUT.

Amplifier stage D1017 can also be switched as an inverter by multiplexer D1008.
This is necessary to correct for the different phases of the two signals in the two sections of the P²CCD.
Presets R1006 and R1024 provide a means of gain adjustment for the two P²CCD sections.
Signal V OUT is applied to conversion unit A8.

6.2.10.4. Control signals generator

In the P-mode, the signals P, PRES, $\overline{\text{FOE}}$ and 78 kHz are converted from TTL to ECL by D1013.
As long as signal PRES = logic 1, these signals control the two D-type flip-flops D1003, which generate the signals WREP and RDEP.

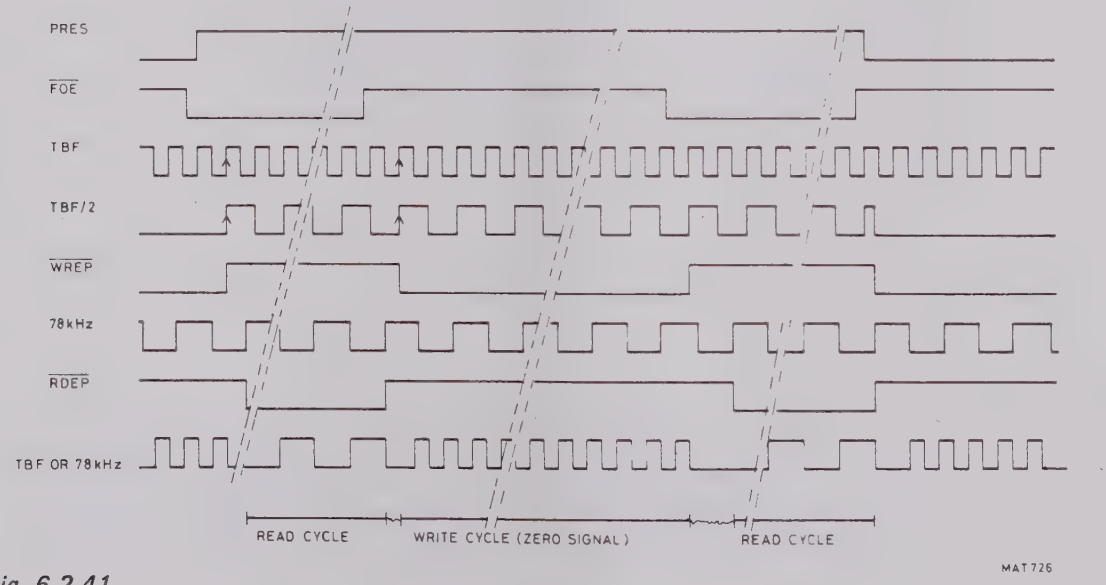


Fig. 6.2.41.

As shown in the timing diagram, during the time that signal $\overline{\text{WREP}}$ = logic 0, new signal samples will be shifted into the P²CCD with a clock-frequency signal derived from signal TBF. (WREP: WRITE ENABLE P-MODE).

Signals WREP and $\overline{\text{WREP}}$ are only switched synchronously with even TBF pulses (TBF/2) in order to achieve precise zero-correction (see ACL unit A9). This is realised by dividing the TBF pulses using the lower flip-flop of D1014, resulting in signal TBF/2, which is used as a clock-signal for flip-flop WREP.

During the time that signal $\overline{\text{RDEP}}$ = logic 0, the P²CCD contents are shifted out with a clock-frequency derived from signal 78 kHz.

Signals RDEP and $\overline{\text{RDEP}}$ are only switched synchronously with the 78 kHz signal.
(RDEP: READ ENABLE P-MODE).

The signal on pin 10 of NOR-gate D1004 is built up by TBF or 78 kHz.
This signal, which is applied to pin 6 of D1006, is also inverted by D1004 and applied to pin 11 of D1006. These flip-flops and the associated circuits that follow (D1007, D1012) generate the signals listed below in accordance with the timing diagram.

RES1:	Reset signal for P2CCD output section I
RES2:	Reset signal for P2CCD output section II
P DRIVE:	P2CCD phase signal
PDR1 & PDR2:	Control signals for multiplexers D1018, D1019 and D1008
CLKDR:	Drive signal for clock-pulse generator.

Integrated circuits D1012 are ECL/TTL converters of which one output is connected to an internal reference voltage of −1,2 V.

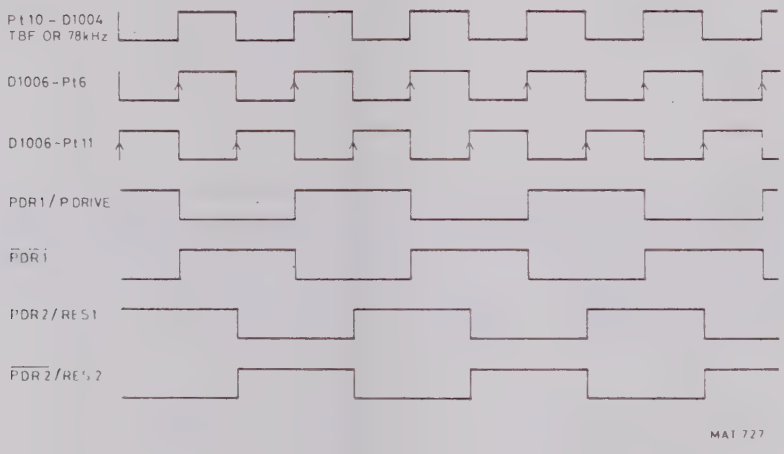


Fig. 6.2.42.

The whole system is inactive while signal $\overline{\text{PECL}}$ from the time-base unit is at logic 1. Signal P DRIVE will then be permanently at logic 1.
Furthermore, the generation of signals PDR1, PDR2, $\overline{\text{PDR2}}$, PDRIVE, RES1 and RES2 is inhibited while signal WREP is at logic 1. This signal is at logic 1 during the reading of new signal samples into the P2CCD. Signals RES1 and RES2 are then positive to open the reset FET during reading in.

Signal HOCONP (Hold and Convert in P-mode)

HOCONP pulses are only generated during the reading of the P2CCD contents. These pulses are derived from the 78 kHz pulses via NOR-gate D1004 while signal $\overline{RDEP}$ = logic 0 (RDEP: READ ENABLE in P-MODE). Immediately the first P2CCD signal sample is available for conversion to digital, the leading edge of the first HOCONP pulse has already passed. Therefore, this analog-to-digital conversion has to be started on the second HOCONP pulse.
For this reason, the first HOCONP pulse is suppressed by the upper flip-flop of D1014 as shown in the following diagram.

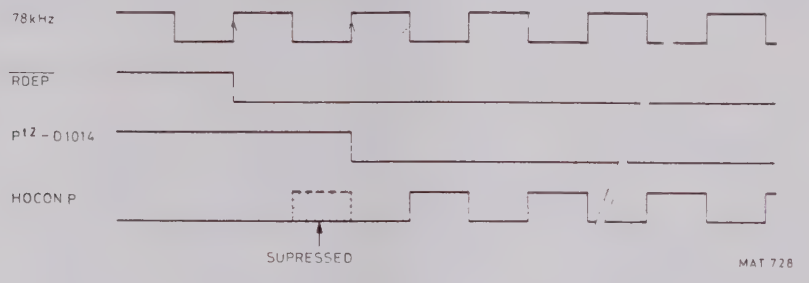


Fig. 6.2.43.

6.2.10.5. Clock-pulse generator

The four clock-pulse signals P2, A2, P1 and A1 needed to shift the signal samples through the P2CCD, are produced by clock-pulse generator D1001 in combination with the LC filters on unit A11, which are terminated by 50 Ω resistors to minimise reflections. One of these double-T filters is connected between the output pins 7 and 6, and the other between the output pins 9 and 10 of clock-pulse generator D1001.
The resulting four square-wave clock-pulse signals have a high level of +11,4 V and a low level of +2 V as shown below.

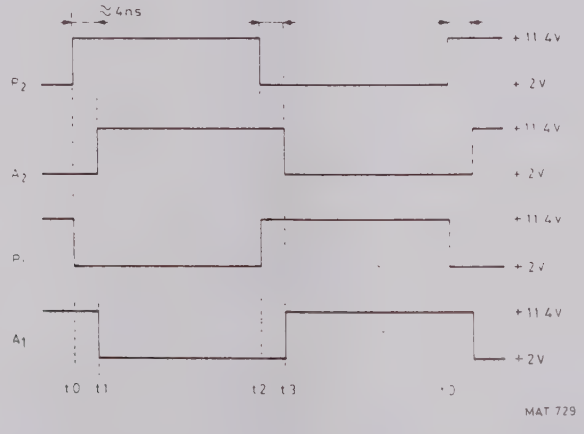


Fig. 6.2.44.

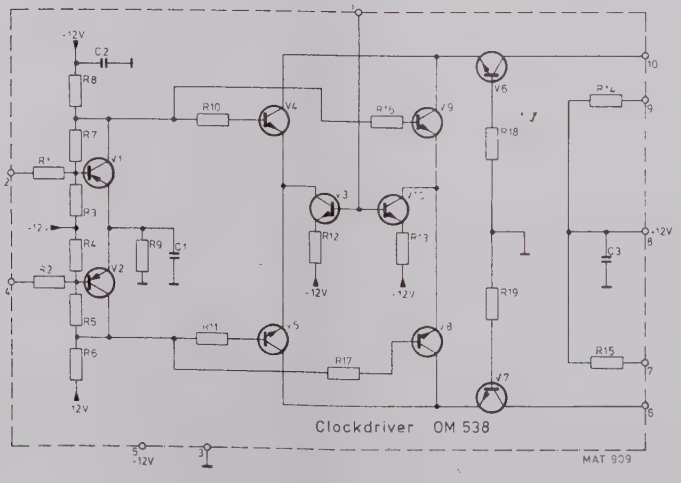


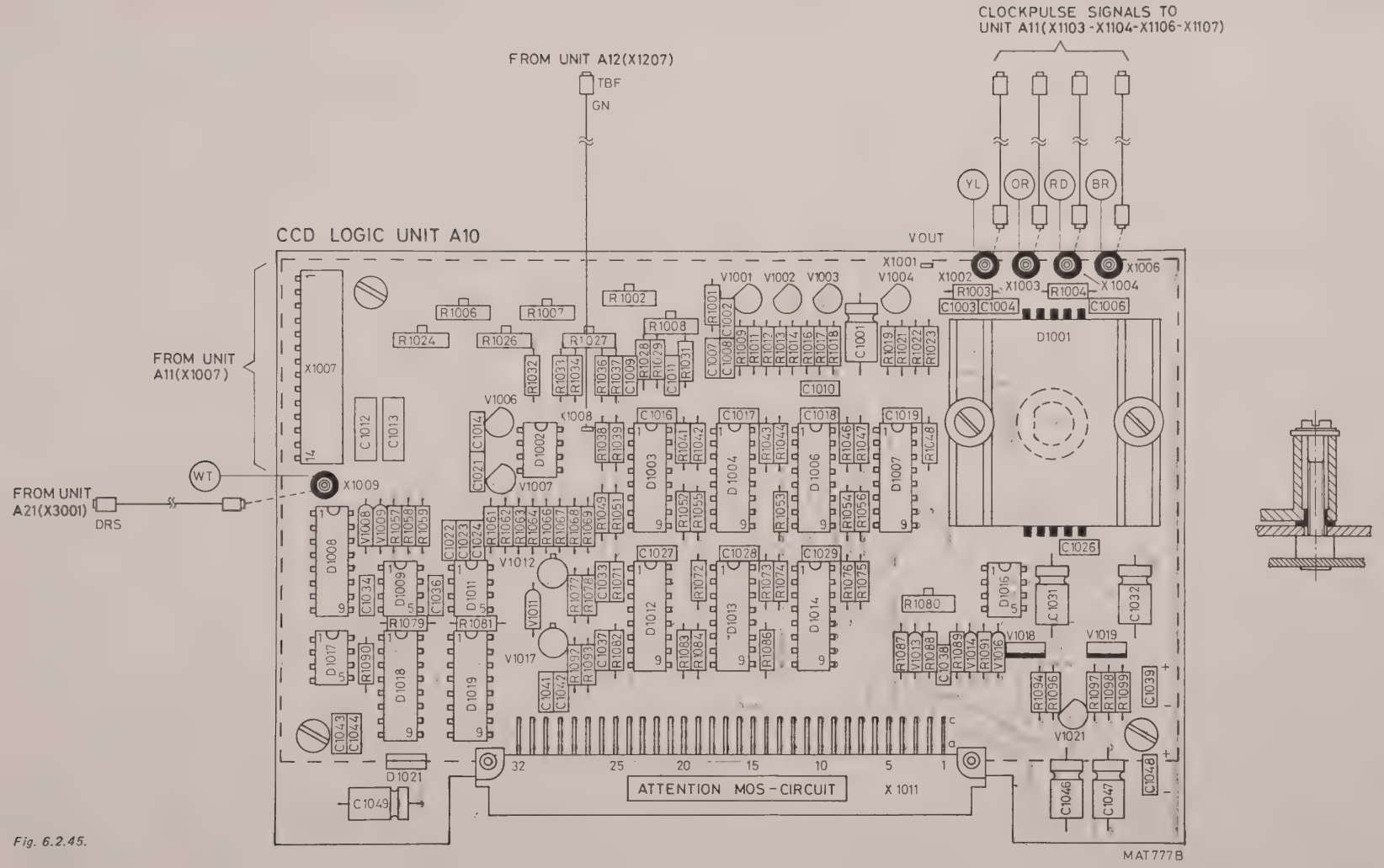
Fig. 6.2.44a

Signals P2/A2 are 180° phase-shifted with P1/A1. The delay between the filter sections is approximately 4 nsec.

For correct sampling of the input signal by the P²CCD, it is necessary that the low level (+2 V) of the clock signals P2 and P1 remains constant. To achieve this, the clock-signals P2 and P1 are measured on unit 10, which results in a feedback signal CLAFB of approximately +3,6 V (clock-pulse amplitude feedback signal).

This voltage is applied to the base of transistor V1001 via low-pass filter R1001/C1002. A stable reference voltage of +3,6 V is applied to the base of transistor V1003. In this way, variations of the low level (+2 V) of the clock-signals P2 and P1 result in a variation of the signal level on the collector of transistor V1003. This variation is then fed back via emitter-follower V1004 to a current source pin 1 of the clock-pulse generator D1001.
The clock-pulse generator is driven by a signal CLKDR from pin 2 of flip-flop D1006.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	BIAS	A10	A11	Bias voltage
CLAFB		A11		Clock-pulse amplitude feedback
	DRAIN	A10	A11	Drain voltage
$\overline{\text{FOE}}$		A9		Frequency output enable
OUTPA		A11		P²CCD output signal section I
OUTPB		A11		P²CCD output signal section II
P		A12		P-mode signal
$\overline{\text{PECL}}$		A12		P-mode signal for ECL circuits
PRES		A9		Enable signal in P-mode
	P11 IN	A10	A11	Threshold voltage
	P22 IN	A10	A11	Threshold voltage
	RES1	A10	A11	Reset signal 1
	RES2	A10	A11	Reset signal 2
	SUB	A10	A11	Substrate voltage
78 kHz		A12		78 kHz pulse
	+11,4 V	A10	A11	
	+40 V	A10	A11	
−5,2 V		A15		
+6 V		A15		
−6 V		A15		
+12 V		A15		
−12 V		A15		
+40 V		A15		
DRS		A21		Signal from T & H gate
TBF		A12		Time-base fast
	VOUT	A10	A8	CCD logic unit analog output signal
	HOCONP	A10	A9	Hold and convert in P-mode


CLOCKPULSE SIGNALS TO
UNIT A11(X1103-X1104-X1106-X1107)
FROM UNIT A12(X1207)
TBF
GN
YL
OR
RD
BR
CCD LOGIC UNIT A10
VOUT
X1001
X1002
X1003
X1004
X1006
FROM UNIT
A11(X1007)
X1007
FROM UNIT
A21(X3001)
DRS
WT
X1009
X1008
D1001
D1002
D1003
D1004
D1006
D1007
D1008
D1009
D1011
D1012
D1013
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C1039
C1046
C1047
C1048
C1049
R1001
R1002
R1003
R1004
R1006
R1007
R1008
R1024
R1026
R1027
R1080
R1079
R1081
ATTENTION MOS-CIRCUIT
X 1011
32
25
20
15
10
5
1
MAT 777 B

Fig. 6.2.45.

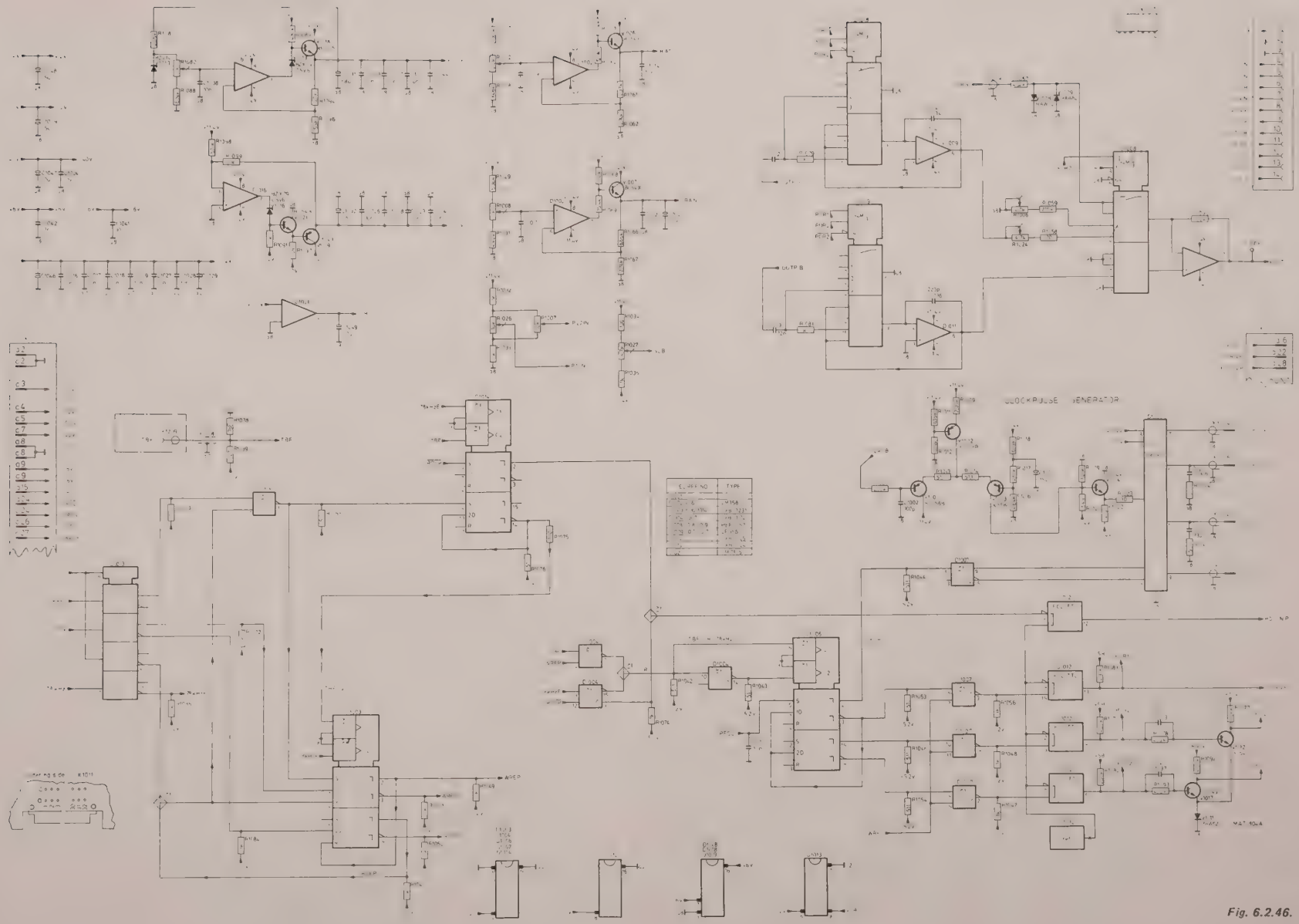


Fig. 6.2.46.

6.2.11. P²CCD unit A11

6.2.11.1. General

The P²CCD circuit (Profiled Peristaltic Charged Coupled Device) is used in this digital storage oscilloscope as an analog shift register. Using this circuit, different time conversions can be realised in the TIME/DIV switch positions 500 ns/DIV up to 0,2 ms/DIV to digitise fast input signals with a relatively slow (12,8 μs approx.) analog-to-digital converter.
The P²CCD circuit D1101 located on unit A11 consists of two CCD sections in parallel. These two sections are required in order to take samples of the input signal on the 0° phase and on the 180° phase of the clock signal.

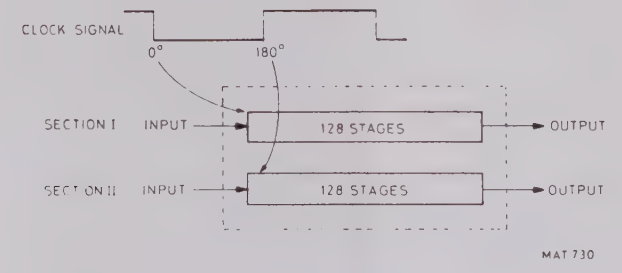


Fig. 6.2.47.

Each section consists of 128 stages, i.e. the complete circuit D1101 contains 256 stages in which a total of 256 samples can be stored.
In addition, each section consists of a system for the transport of charges, an input circuit that accepts the charges from the vertical channel switch signals P AMP OUT I and P AMP OUT 2, and an output section which measures the sizes of the charges and produces corresponding output signals.

Samples can be taken from the analog input signal at a high sample rate, which varies between 125 kHz and 50 MHz depending on the TIME/DIV switch setting. These samples are shifted into the P²CCD.

After the reading in of information in all the 256 stages, the reading out cycle is started. The entire operation is carried out under the control of the acquisition control logic and the CCD logic unit.

The P²CCD circuit contents are read out with a lower frequency of 78 kHz approx.
This frequency remains the same for the different TIME/DIV switch settings and is low enough to guarantee perfect ADC conversion by the ADC on unit A8.
The frequency must not be too low otherwise loss of information could occur in the P²CCD circuit.

6.2.11.2. Input section

Each of the two sections of the P2CCD circuit has its own input section. One of these input sections is now described. This particular section has the following inputs:

IN1 (pin 22) — this input is connected to the clock signal P2 in such a way that the d.c. voltage level on IN1 is always about 13 V more positive than the P2 signal level.

P11IN (pin 21) — this is a threshold voltage set to +6 V approx.

A11IN (pin 17) — this is connected to the analog input signal P AMP OUT 1 with a maximum amplitude of 1 V peak-peak on a d.c. bias level of about +7,5 V.

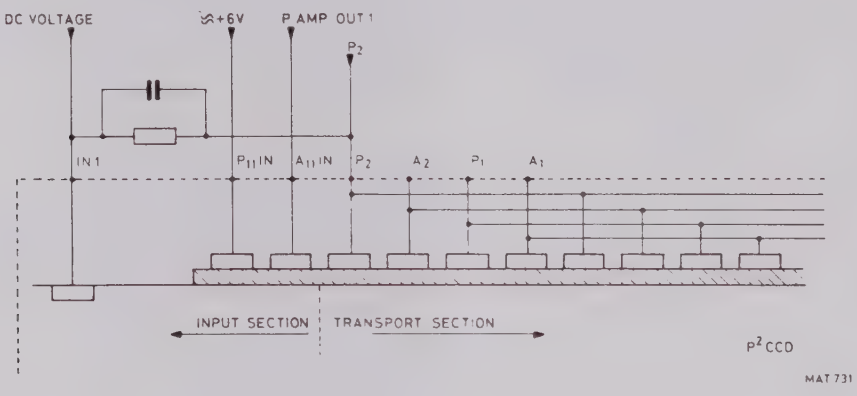


Fig. 6.2.48.

For correct sampling of the input signal, it is most important that the low level (+2 V) of the clock signal P2 remains constant. For higher frequencies, the amplitude of the clock signal P2 decreases due to the capacitive loading caused by the P2CCD circuit.
A control loop is used to ensure that the low level of P2 remains constant.
The clock signals P2 and P1 are measured by the circuit V1101, V1117, which results in a feedback signal CLAFB for the four-phase clock-pulse generator on unit A10.
(CLAFB = CLOCK AMPLITUDE FEEDBACK).

6.2.11.3. Transport section

The four clock signals P2, A2, P1 and A1 are used to shift information in and out of the P2CCD. These signals, generated on CCD logic unit A10, are derived from the 125 kHz ... 50 MHz input frequency (TBF) from the time-base circuit (A12) when reading in, and from a 78 kHz input frequency when reading out.

Each stage inside the P2CCD consists of four gates that are isolated from each other, and are controlled by the four clock signals as shown in the following diagram.

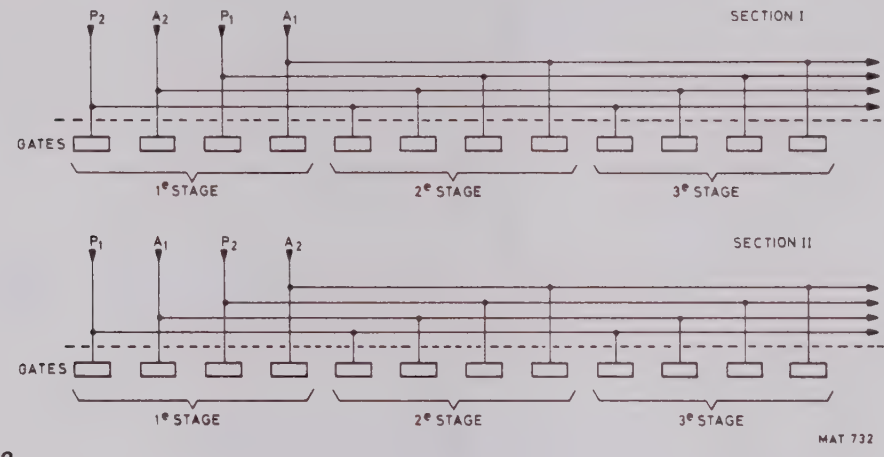


Fig. 6.2.49.

The charges are transported in the following way:

Assume for instance that a negative charge is brought under a positive gate. If the next gate is made positive and the previous gate is made negative, the charge will be repelled in the direction of the position gate.

Displacement of charges is achieved in practice by changing the levels on the gates by the four periodically changing clock-pulses. For a description of the clock-pulse generator, refer to unit A10.

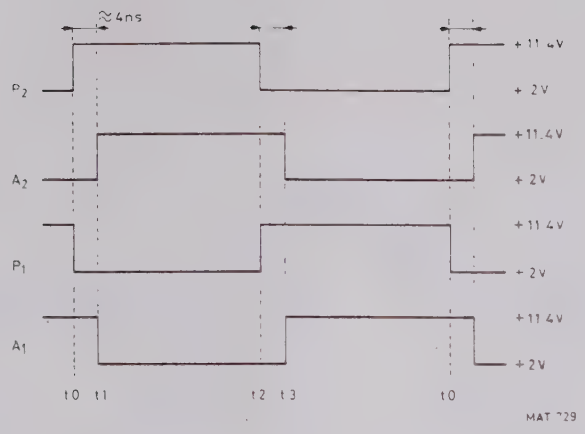


Fig. 6.2.50. Timing clock signals

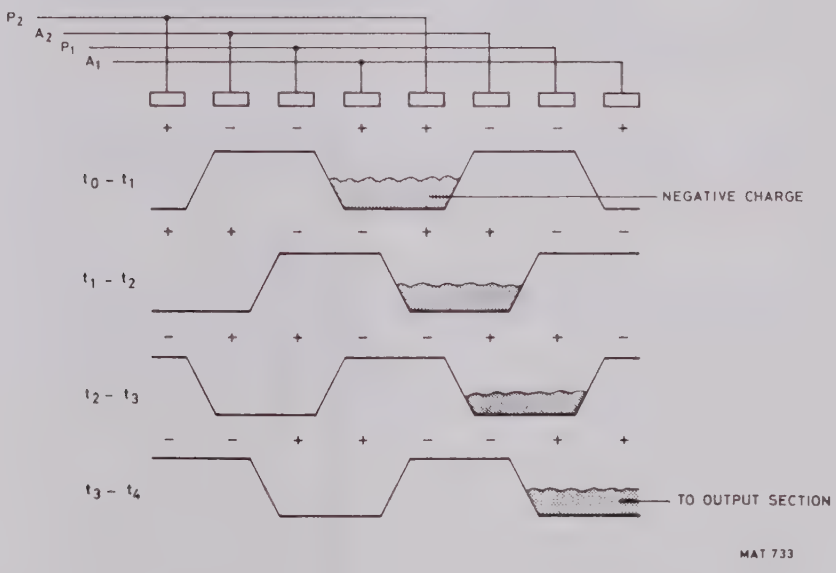


Fig. 6.2.51. Displacement of a negative charge as a function of the clock voltages.

6.2.11.4. Output section

Each of the two P2CCD sections has its own output stage, as now described.

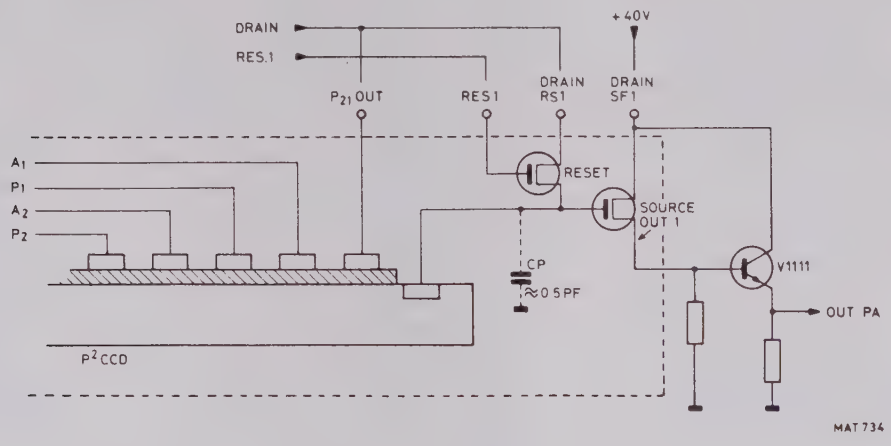


Fig. 6.2.52.

On every positive-going edge of the clock signal A1 a charge will load the parasitic capacitor C_p of the source-follower gate (previously discharged to the DRAIN RS1 voltage level by the reset FET).

The level across C_p will leave the output section via the appropriate source-follower. Both FET transistors are also part of the P2CCD circuit.
The output signal is approx. 100 mV for an input signal (Vin) of 1 Vp-p.
This source-follower output signal is applied to an emitter-follower V1111 which in turn feeds it as signal OUTPA to an output amplifier on unit A10.

6.2.11.5. P2CCD circuit in dual-channel mode

In the dual-channel mode, channel A signal is shifted to section I and channel B to section II. The clock signals for the two sections are in anti-phase, which results in a situation where the P2CCD itself acts as a chopper.
The chopper frequency depends on the TIME/DIV switch setting.
This dual-mode of working results in 128 samples per channel being stored, instead of 256.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
BIAS		A10		Bias voltage
	CLAFB	A11	A10	Clock-pulse amplitude feedback
DRAIN		A10		Drain voltage
	OUTPA	A11	A10	P2CCD output signal section I
	OUTPB	A11	A10	P2CCD output signal section II
P11IN		A10		Threshold voltage
P22IN		A10		Threshold voltage
RES1		A10		Reset signal 1
RES2		A10		Reset signal 2
SUB		A10		Substrate voltage
+11,4 V		A10		
+40 V		A10		
PAMPOUT1		A21		Output signal of amplifier
PAMPOUT2		A21		Output signal of amplifier

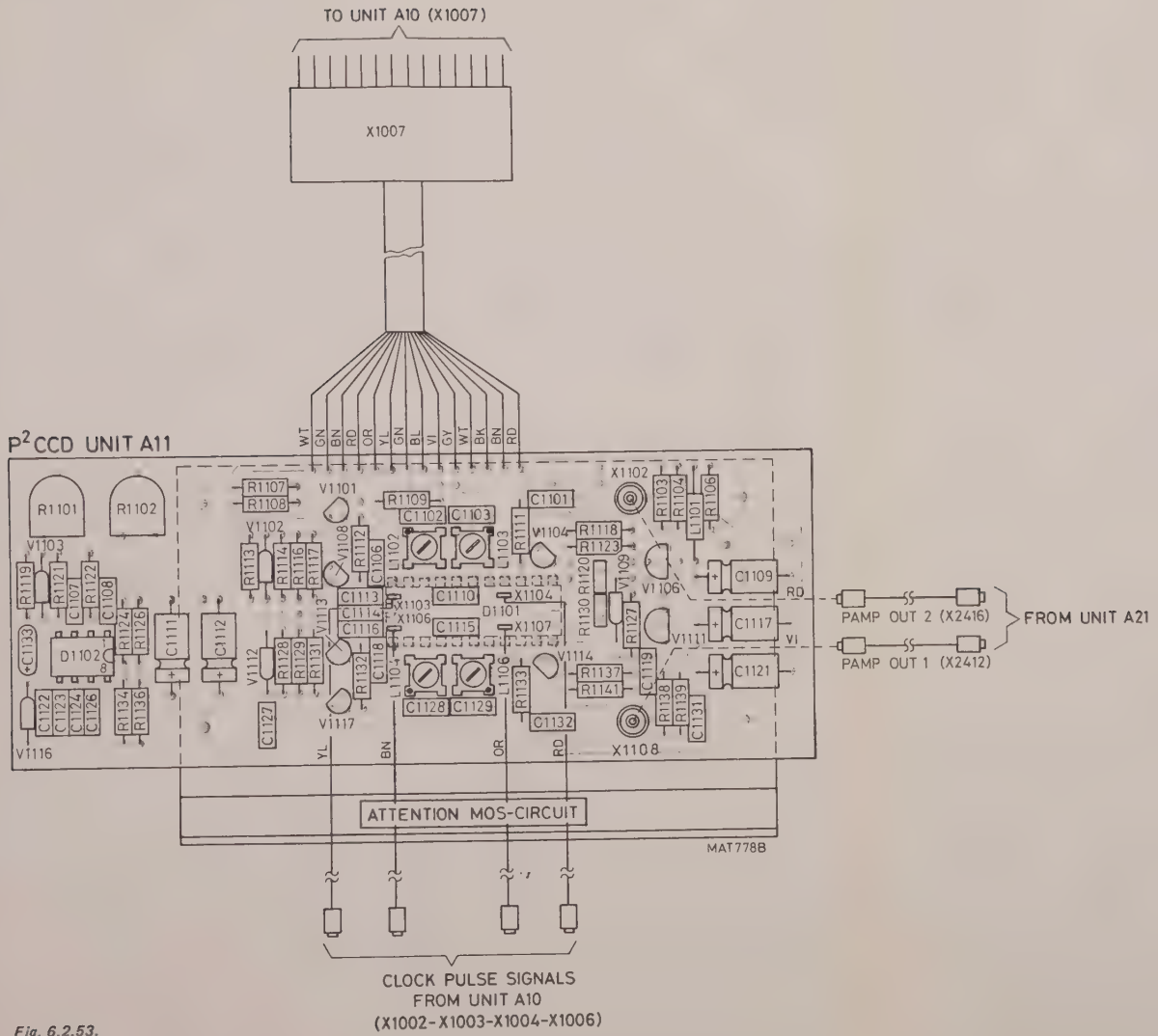
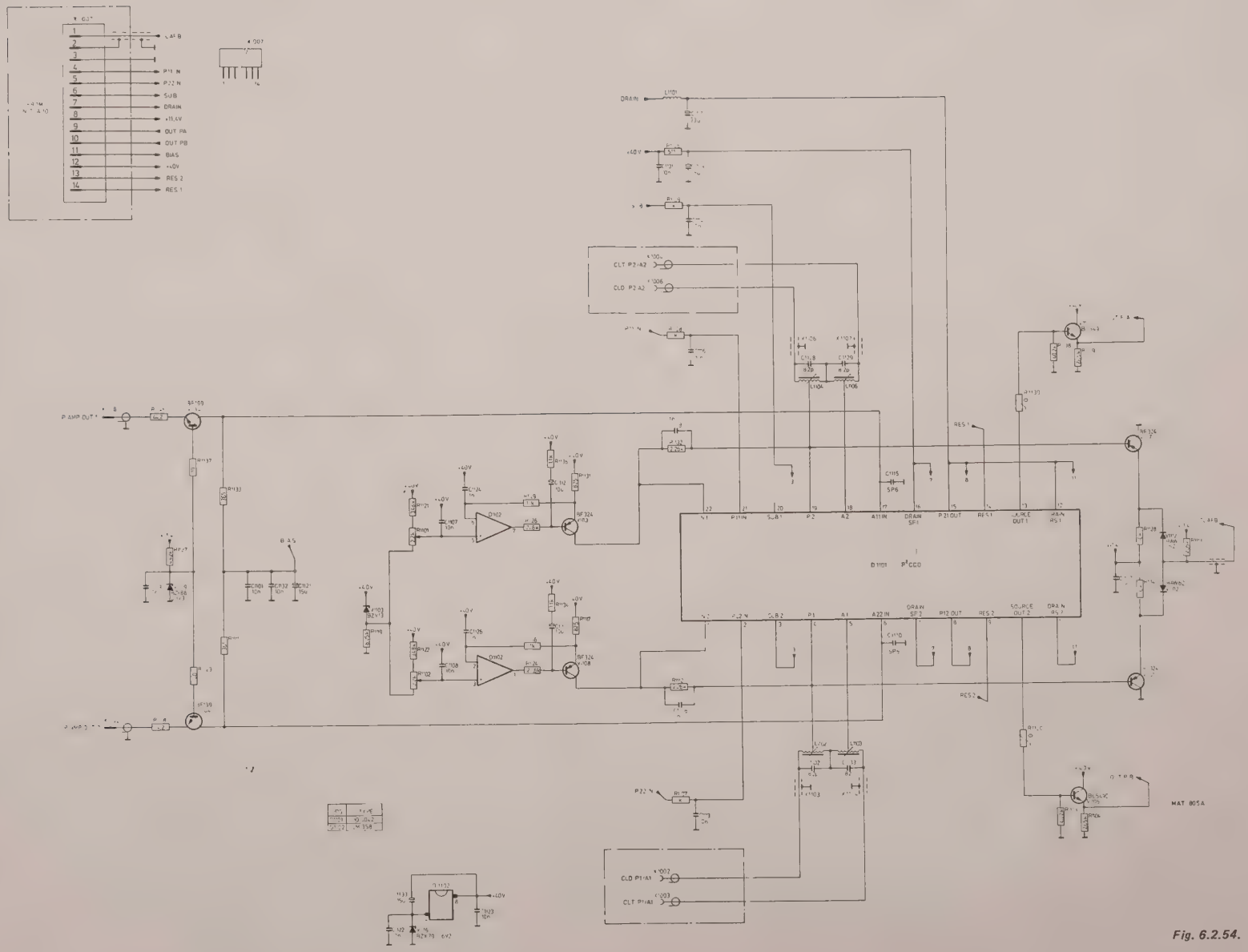

TO UNIT A10 (X1007)
X1007
WT GN BN RD OR YL GN BL VI GY WT BK BN RD
P2 CCD UNIT A11
R1101
R1102
V1103
R1119
R1121
C1107
R1122
C1108
C1133
D1102
R1124
R1126
C1111
C1112
C1122
C1123
C1124
C1126
R1134
R1136
V1116
R1107
R1108
V1101
V1102
R1113
R1114
R1116
R1117
V1108
R1112
C1106
L1102
R1109
C1102
C1103
L1103
R1111
C1101
V1104
R1118
R1123
X1102
R1103
R1104
L1101
R1106
R1120
R1130
V1109
V1106
C1109
RD
C1113
C1114
C1116
X1103
X1106
C1110
X1104
D1101
C1115
X1107
R1127
V1111
C1117
VI
V1112
R1128
R1129
R1131
V1113
R1132
C1118
L1104
C1128
C1129
L1106
R1133
V1114
R1137
R1141
C1119
C1121
C1127
V1117
C1132
R1138
R1139
C1131
X1108
YL
BN
OR
RD
PAMP OUT 2 (X2416)
PAMP OUT 1 (X2412)
FROM UNIT A21
ATTENTION MOS-CIRCUIT
MAT778B
CLOCK PULSE SIGNALS
FROM UNIT A10
(X1002-X1003-X1004-X1006)

Fig. 6.2.53.



DRAIN
+40V
CLT P2/A2
CLD P2/A2
P AMP OUT 1
BIAS
D1101 P²CCD
CLD P1/A1
CLT P1/A1
MAT 805A

Fig. 6.2.54.

6.2.12. Time-base unit A12

The time-base unit generates a number of control signals of different frequencies derived from the microprocessor clock-pulse output signal of 2,5 MHz.

6.2.12.1. Encoding TIME/DIV settings

Depending on the setting of the TIME/DIV switch, one of these frequencies is selected and applied to other units as signals TBF (time-base fast, used in P²CCD mode) or TBS (time-base slow, used for other modes).

The relation between the TIME/DIV switch settings and the signals TBF and TBS is such that there are always 25 pulses (TBF or TBS) generated per horizontal division.

The settings of the TIME/DIV switch are read by the microprocessor system (unit A2).
The microprocessor loads the 8-bit latch D1221 with a byte of data according to the TIME/DIV settings listed in the following table.
Latch D1221 is selected when the microprocessor generates address 8Ø6ØH.
When the microprocessor places this address on the address bus, signal $\overline{IO6}$ goes to logic 0.
This $\overline{IO6}$ signal combined with the $\overline{WR}$ signal enables data latch D1221 to latch the data present on the data bus.

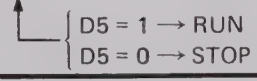
The output signals of latch D1221 have the following functions:

DØ ... D4* — used to control the various multiplexers on time-base units A12.

D5* — enables or disables the output signal TBS.

D6* and D7* — these signals together, control decoder D1216, which results in the four mode signals:
- P – P²CCD mode
- D – Direct mode
- R – Roll mode
- S – Sampling mode

TIME/DIV	FREQUENCY	MODE	D7	D6	D5	D4	D3	D2	D1	DØ
5 ns/div		S	1	1	0	0	0	1	1	0
10 ns/div		S	1	1	0	0	0	0	0	1
20 ns/div		S	1	1	0	0	0	1	0	0
50 ns/div		S	1	1	0	0	0	1	0	1
0.1 µs/div		S	1	1	0	0	0	0	0	0
0.2 µs/div		S	1	1	0	0	0	1	1	1
	TBF									
0.5 µs/div	50 MHz	P	0	0	0	0	1	1	0	1
1 µs/div	25 MHz	P	0	0	0	0	1	1	1	0
2 µs/div	12,5 MHz	P	0	0	0	0	1	0	1	0
5 µs/div	5 MHz	P	0	0	0	0	1	0	1	1
10 µs/div	2.5 MHz	P	0	0	0	1	0	0	0	1
20 µs/div	1.25 MHz	P	0	0	0	1	0	0	1	0
50 µs/div	0.5 MHz	P	0	0	0	1	0	0	1	1
0.1 ms/div	0.25 MHz	P	0	0	0	1	1	0	0	1
0.2 ms/div	125 kHz	P	0	0	0	1	1	0	1	0
	TBS									
0.5 ms/div	50 kHz	D	1	0	1	0	0	0	0	0
1 ms/div	25 kHz	D	1	0	1	0	0	0	0	1
2 ms/div	12.5 kHz	D	1	0	1	0	0	0	1	0
5 ms/div	5 kHz	D	1	0	1	0	0	1	0	0
10 ms/div	2.5 kHz	D	1	0	1	0	0	1	0	1
20 ms/div	1.25 kHz	D	1	0	1	0	0	1	1	0
50 ms/div	500 Hz	D	1	0	1	0	1	0	0	0
0.1 s/div	250 Hz	D	1	0	1	0	1	0	0	1
0.2 s/div	125 Hz	D	1	0	1	0	1	0	1	0
	TBS									
0.5 s/div	50 Hz	R	0	1	0/1	0	1	1	0	0
1 s/div	25 Hz	R	0	1	0/1	0	1	1	0	1
2 s/div	12.5 Hz	R	0	1	0/1	0	1	1	1	0
5 s/div	5 Hz	R	0	1	0/1	1	0	0	0	0
10 s/div	2.5 Hz	R	0	1	0/1	1	0	0	0	1
20 s/div	1.25 Hz	R	0	1	0/1	1	0	0	1	0
30 s/div	5/6 Hz	R	0	1	0/1	1	0	1	0	0
60 s/div	5/12 Hz	R	0	1	0/1	1	0	1	0	1
120 s/div	5/24 Hz	R	0	1	0/1	1	0	1	1	0
360 s/div	5/72 Hz	R	0	1	0/1	1	1	0	0	0
900 s/div	5/180 Hz	R	0	1	0/1	1	1	1	0	1
1800 s/div	5/360 Hz	R	0	1	0/1	1	1	1	1	0
3600 s/div	5/720 Hz	R	0	1	0/1	1	1	1	1	1



6.2.12.2. Generation of signals 1.25 MHz, 0.5 MHz, 250 kHz, 156 kHz, 78 kHz

The 2.5 MHz clock-pulse signal from the microprocessor is divided by factors of 2, 5 and 10 in divider D1206, resulting in signals 1,25 MHz (pin 3), 0.5 MHz (pin 4) and 250 kHz (pin 6) respectively.

Two other signals are derived from the 1.25 MHz signal by D1207, which divides by factors of 8 and 16. These divisions produce a signal of 156 kHz for use in the Z-amplifier and a signal of 78 kHz for reading out the contents of the P^2CCD unit.

6.2.12.3. Generation of TBS signals for the D and R modes

The 0.5 MHz signal on pin 4 of D1206 is applied to pin 10 of D1206, the first of a chain of dividers consisting of D1206, D1204, D1203, D1202 and D1201.
The first three of these divide by a factor of ten, thus producing the frequencies 50 kHz, 5 kHz, 500 Hz, 50 Hz and 5 Hz.
The 2.5 kHz output from D1204 pin 11 is applied via inverter D1218 (8, 9, 10) to the final amplifier unit A20 for generating the CAL voltage.

Pin 2 of D1203, normally at 500 Hz, can be switched to 2.5 MHz by switch S1201 for test purposes in the ROLL-Mode.

Circuit D1202 divides the 5 Hz input signal by a factor of 6 to give an output signal with a frequency of 5/6 Hz. In turn, D1201 divides this 5/6 Hz input signal by a factor of 12 if D2* is logic 0, and by a factor of 15 if D2* is logic 1, thus producing frequencies of 5/72 Hz or 5/90 Hz.

All these frequencies are routed to multiplexer D1214, the outputs of which are controlled by signals D2*, D3* and D4*.
Only one of the input frequencies appears on output 3 of D1214 and is applied in one of two ways to multiplexer D1219:

- directly to input 6 of D1219, or
- first divided in D1207 by factors of 2, 4 and 8 and then applied to inputs 5, 4 and 3 of D1219.

Multiplexer D1219 is controlled by signals DØ* and D1*.
The final selected frequency, obtained via NOR-gate D1217 as signal TBS, is applied to the trigger unit.
The output TBS can be disabled by flip-flop D1222, under the control of the D5* signal.
Signal TBS is blocked at the end of the ROLL-mode and in the P-mode. D* is then logic 0.

6.2.12.4. Generation of TBF signals for the P-mode

Signals of a higher frequency than the microprocessor clock-pulse output signal of 2.5 MHz are generated by means of a voltage-controlled oscillator (VCO) D1213 that has an output frequency of 100 MHz.
The output frequency of this oscillator is controlled by a d.c. voltage, VC_X on the VCO input, pin 2.
To obtain this stable VCO output, the 100 MHz output is divided by a factor of 80 in circuits D1227, D1209 and D1208. The resulting 1.25 MHz signal, VCO/80, is then compared with a reference signal of the same frequency in a phase detector, which is then used to control the VCO frequency.

The phase detector comprises the flip-flops D1211 and the associated integrator circuit. These flip-flops are set and reset in accordance with the timing diagram shown below.
The output signals on pins 1 and 12 are added and applied to pin 2 of D1212 of the integrator. The resulting signal VC_X controls the VCO to ensure a constant frequency. The VCO is only switched into circuit by signal VCOEN (VCO Enable) in the 4 TIME/DIV switch positions 0.5 µs/div to 5µs div.

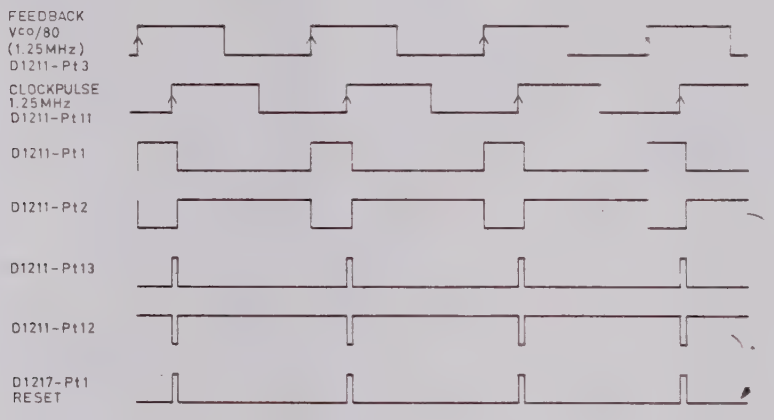


Fig. 6.2.55.

Divider D1227 derives the 50 MHz and 25 MHz signals from the 100 MHz VCO output signal, these being routed to multiplexer D1224 for selection.
The 25 MHz signal is also applied to a multiplexer D1223 via ECL/TTL converter D1231. This multiplexer selects one of the input signals 25 MHz, 2.5 MHz and 250 kHz under the control of signals D3* and D4*.

The 25 MHz output signal from D1223 is divided in D1209 by a factor of 5 and a factor of 2. From there it is divided further in D1208 by a factor of 2, giving a signal VCO/80 of 1.25 MHz on output pin 12 of D1208. This is the 1.25 MHz signal that is fed back to the phase detector for controlling the VCO frequency.

The following frequencies are also available:

output pin 9 of D1223: 25 MHz, 2.5 MHz or 250 kHz
output pin 8 of D1222: 12,5 MHz, 1.25 MHz or 125 kHz
output pin 12 of D1209: 5 MHz, 500 kHz (or 50 kHz - not used)

After selection by multiplexer D1219 (only enabled in P-mode), one of these frequencies appear on output pin 9 of D1219.

The selected signal is applied to multiplexer D1224 via a TTL/ECL converter, D1225.

Multiplexer D1224, which is controlled by DØ*, D1* and D2*, is employed for the final selection of the frequency of the output signal TBF. This signal is applied to the CCD logic unit A10 via a 50 Ω cable.
In parallel, a TBF signal is generated, which is connected via a 50 Ω cable to the trigger unit A22.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	D	A12	A9	DIRECT-mode signal
DØ ... D7		A4		Data bits from system data bus
$\overline{IO6}$		A4		Address decoding signal TB select
	R	A12	A9	ROLL-mode signal
	S	A12	A9-A22	SAMPLE-mode signal
	P	A12	A7-8-9-10-21	P^2CCD-mode signal
	$\overline{PECL}$	A12	A10	P-mode signal from ECL circuits
	TBF CCD	A12	A10	Time-base fast for CCD unit
	TBF TRIGGER	A12	A13	Time-base fast for TRIGGER unit
	TBS	A12	A13-A22	Time-base slow signal
	50 kHz	A12	A9	
	78 kHz	A12	A10	
	2.5 kHz	A12	A20	2.5 kHz for CAL voltage
	156 kHz	A12	A15	
	1.25 MHz	A12	A9-13	
$\overline{WR}$		A4		Signal WRITE from microprocessor
2.5 MHz		A4		Microprocessor clock-pulse output signal
+5 V		A15		
–5.2 V		A15		

TEST POINTS	
X1201	RESET
X1202	LOW
X1203	5 Hz
X1204	156 kHz
X1207	TBF
X1208	VC_X

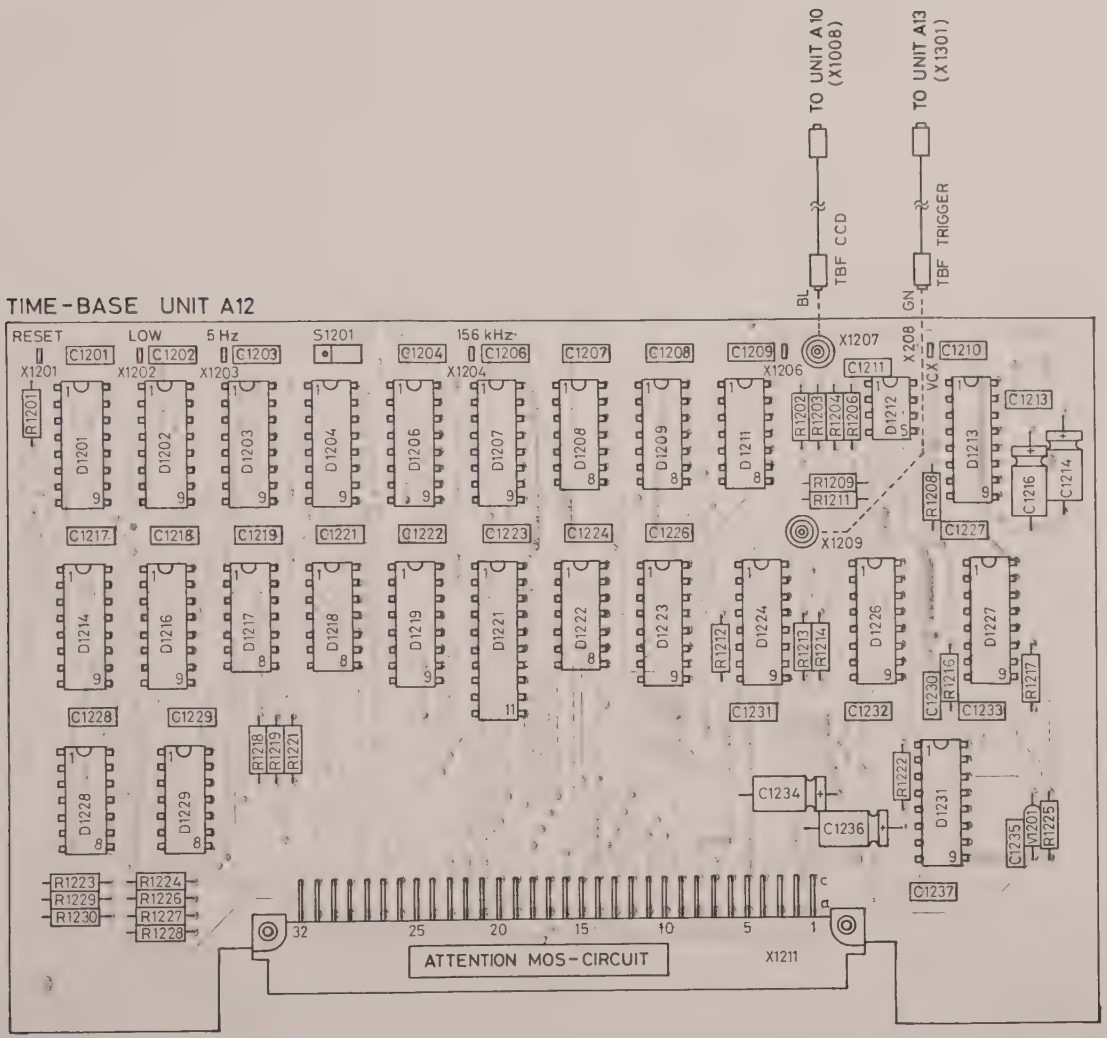


Fig. 6.2.56.

MAT 779B

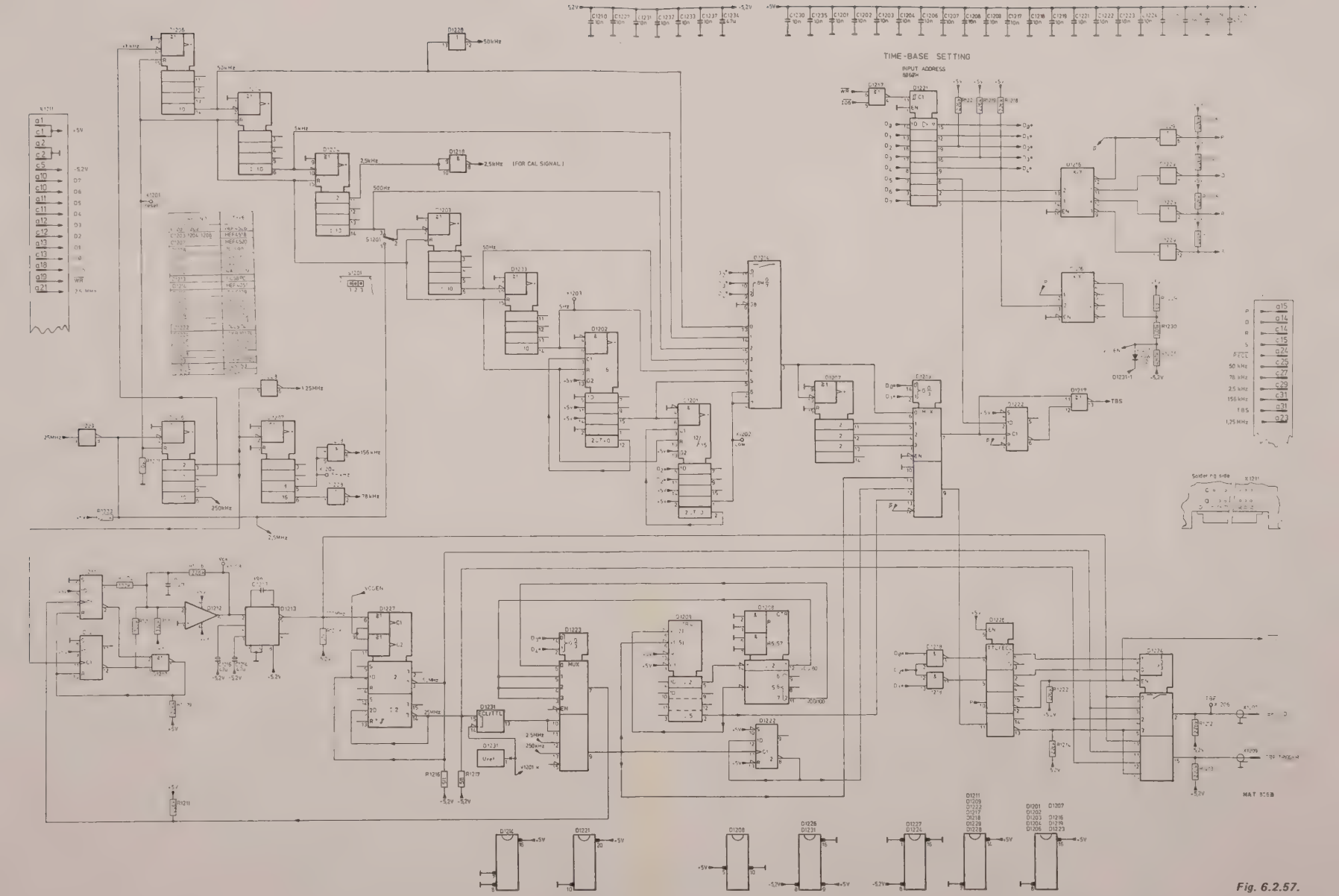

TIME-BASE SETTING
INPUT ADDRESS
886FH
50kHz
5kHz
2.5kHz
2.5kHz (FOR CAL SIGNAL)
500Hz
50Hz
1.25MHz
250kHz
2.5MHz
156 kHz
78 kHz
TBS
MAT 856B

Fig. 6.2.57.

6.2.13. Delay trigger unit A13

The delay trigger unit comprises the following sub-circuits:

- The time-base AUTO circuit
- Plot output circuit and control signals for the dot-join circuit
- Down counters for trigger delay in Direct or P2CCD mode
- Digital-to-analog converter for trigger delay in Sampling mode

6.2.13.1. The time-base AUTO circuit

The time-base auto circuit consists of D1321 and its associated components. In the absence of the TRIST signal, i.e. no trigger pulse, and with the trigger switch in the AUTO mode, the trigger flip-flop of the ACL unit A9 requires a pulse to restart. This pulse is generated by D1321 output 4 and is referred to as the $\overline{\text{AUTR1}}$ signal.

A FRUN signal can enable the output pulse of the trigger unit A22. If no TRIST pulses are available, the re-triggerable monostable multivibrator D1321 (output 12) is at the rest position with output 12 at logic high. Together with signal AUTOTB, which is also high from the AUTO switch, output 6 of D1313 goes high. This output is the FRUN signal. As this time, D1321 output 4 is enabled and, on receipt of a $\overline{\text{CTF}}$ pulse, the $\overline{\text{AUTR1}}$ signal goes active low for 3 μs approx. to preset the trigger flip-flop on the ACL unit
A frequency of 1,25 MHz is applied at input 1 of D1321 to ensure that an $\overline{\text{AUTR1}}$ pulse occurs.

6.2.13.2. Plot output circuit and control signals for the dot-join circuit

The X OUT and Y OUT signals derived from the final amplifier unit A20 are applied to the sample-and-hold gates D1328 and D1329. At a particular moment, determined by the software, the data line D3 goes high for 30 μs approx. and D1328 and D1329 respectively will now hold the instantaneous values of X OUT and Y OUT for 17 ms approx. The outputs of the sample-and-hold gates are buffered by operational amplifiers D1319 and D1331 to obtain output voltages of 1 V full-scale for X and Y plotting.

The pen-lift circuit is controlled by a high level on data line D4 at the moment that D1318 is enabled. Changeover of the soldered dot-connection between D1323 and R1334 gives the possibility of active high or active low pen-lift operation. The output is an open-collector output with a maximum load capability of 1 A.

The following pulses are all derived from the $\overline{\text{WR}}$ pulse by a network of dividers and logic gates, and serve to control the dot-join circuit (final amplifier A20):
QØ and Q1; ZDJ and RESDJ, and TRSH.
The signals QØ and Q1 control the channel separation. Signal TRSH controls the sample-and-hold gates of the dot-join, the signal RESDJ serving to control the reset dot-join for the X channel. The ZDJ signal generates the blanking pulse on the microprocessor board and discharges the capacitor of the sawtooth generator on the final amplifier unit.

6.2.13.3. Down counters for trigger delay in Direct or P2CCD modes

The input of the counters may be the signal TBF or TBS. Signal TBF is at ECL-level at a frequency of 125 kHz ... 50 MHz. Conversely, the TBS signal is at TTL-level and at a frequency below 125 kHz.
Both signals are always 25 pulses per division. The signal TBS is converted into ECL-level and applied via a wired-OR circuit to D1306, which functions as a divide-by-five circuit (output on pin 15). Via ECL/TTL converter D1307, the signal is applied to the 4-stage down counter consisting of D1308, D1309, D1311 and D1312. This system operates as follows:

The preset trigger delay in the DIV display is converted to a particular number by the microprocessor system and this number is set on the data-bus and loaded in the counters in two cycles.
First, D1308 and D1309 are loaded by enabling them (on D1308-1 and D1309-11) with pulse $\overline{\text{IO8}}$ together with address 8086 and the $\overline{\text{WR}}$ pulse. After this, D1311 and D1312 are loaded by enabling them (pins 11) with pulse $\overline{\text{IO8}}$ in combination with address 8085 and $\overline{\text{WR}}$ pulse.
The number now loaded must be counted down. The count pulses are derived from signals TBS or TBF, which may be enabled by $\overline{\text{EDCT}}$ applied via TTL/ECL converter D1303 and flip-flop D1304 to input 7 of D1306.
The pulse $\overline{\text{EDCT}}$ is generated under the following conditions:

- Reset input 1 of D1317 is high.
- TRIST pulse goes high.

In this event, $\overline{\text{EDCT}}$ goes active, so set input 5 of D1304 goes low, and on receipt of a TBS or TBF pulse at clock input 6 of D1304, output 3 goes high and enables D1306 as a five-counter.
After counting down to zero, output 13 of D1312 goes low and via AND-gate D1316 (8, 9, 10) the reset input 1 of D1317 goes low and output 6, the $\overline{\text{EDCT}}$ pulse, goes high to disable D1306.

Divider D1306 must be blocked during the new loading of the down counter. This is achieved by the pulse NTSC which remains low during loading, and D1317 reset 1 remains low.
After loading, D1317 reset 1 goes high and on receipt of a TRIST pulse, signal $\overline{\text{EDCT}}$ reverts to the active state.
If the counter is blocked, the signal DELTRG goes high via D1323 and D1316 (4, 5, 6).

6.2.13.4. Digital-to-analog converter for trigger delay in Sampling mode

In the sampling mode, an analog signal is required to delay the trigger. This signal is derived from the digital-to-analog converter D1327, which is loaded with the information of the data-bus when enabled by pulse $\overline{\text{WR}}$ in combination with $\overline{\text{IO8}}$ and address 8086.
The digital information is coded by the software and is converted into an analog voltage. This is a d.c. voltage for the time during which no change is made in the delay setting. The total delay possible in the sampling mode is 100 divisions. These 100 divisions are digitally divided into 200 steps; that is, each division delay is digitally two steps. On conversion, it is then 80 mV/division.
The function of the trigger delay is explained in the description of the trigger unit A22.

Note: Bear in mind that the principle of the oscilloscope with a trigger delay of zero means that the DELTRIG pulse always appears 10 divisions after the TRIST pulse.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A0 - A1 - A2		A4		Address bits from system address bus
AUTO TB		A22		Auto signal from AUTO switch
	$\overline{\text{AUTRI}}$	A13	A9	Auto trigger
	$\overline{\text{AVSB}}$	A13	A4-6-20	logic "0" in X= A/Y= B mode
$\overline{\text{CTF}}$		A9		Clear signal for trigger flip-flop
DØ . . . D7		A4		Data bits from system data bus
	DACDEL	A13	A22	Output signal of DAC delay
	DELTRG	A13	A9-A202	Delayed trigger signal
	DJ	A13	A20	Dot join signal
DT		A4		Display timing
	ENKEL	A13	A20	Single channel mode
	FAS DI	A13	A6	Phase on display level
	FRUN	A13	A22-A202	Freerun signal
$\overline{\text{IO8}}$		A4		I/O address decoding signal
	PEN LFT	A13	OUTPUT	Penlift
	Q0 - Q1	A13	A20	Control signals for dot join
	RESDJ	A13	A20	Reset dot join
TBF		A12		Time-base fast
TBS		A12		Time-base slow
TRIST		A22		Trigger signal for strecher
	TRSH	A13	A20	Trigger for dot join sample & hold
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
X OUT		A20		Horizontal output signal
	X PLOT	A13	OUTPUT	Horizontal plot output signal
	Y EX	A13	A20	Y-expand
Y OUT		A20		Vertical output signal
	Y PLOT	A13	OUTPUT	Vertical plot output signal
	ZDJ	A13	A4-A20	Z dot join
1.25 MHz		A12		
2.5 MHz		A4		
+5V		A15		
−5.2V		A15		
+12V		A15		
−12V		A15		
⊥		A15		

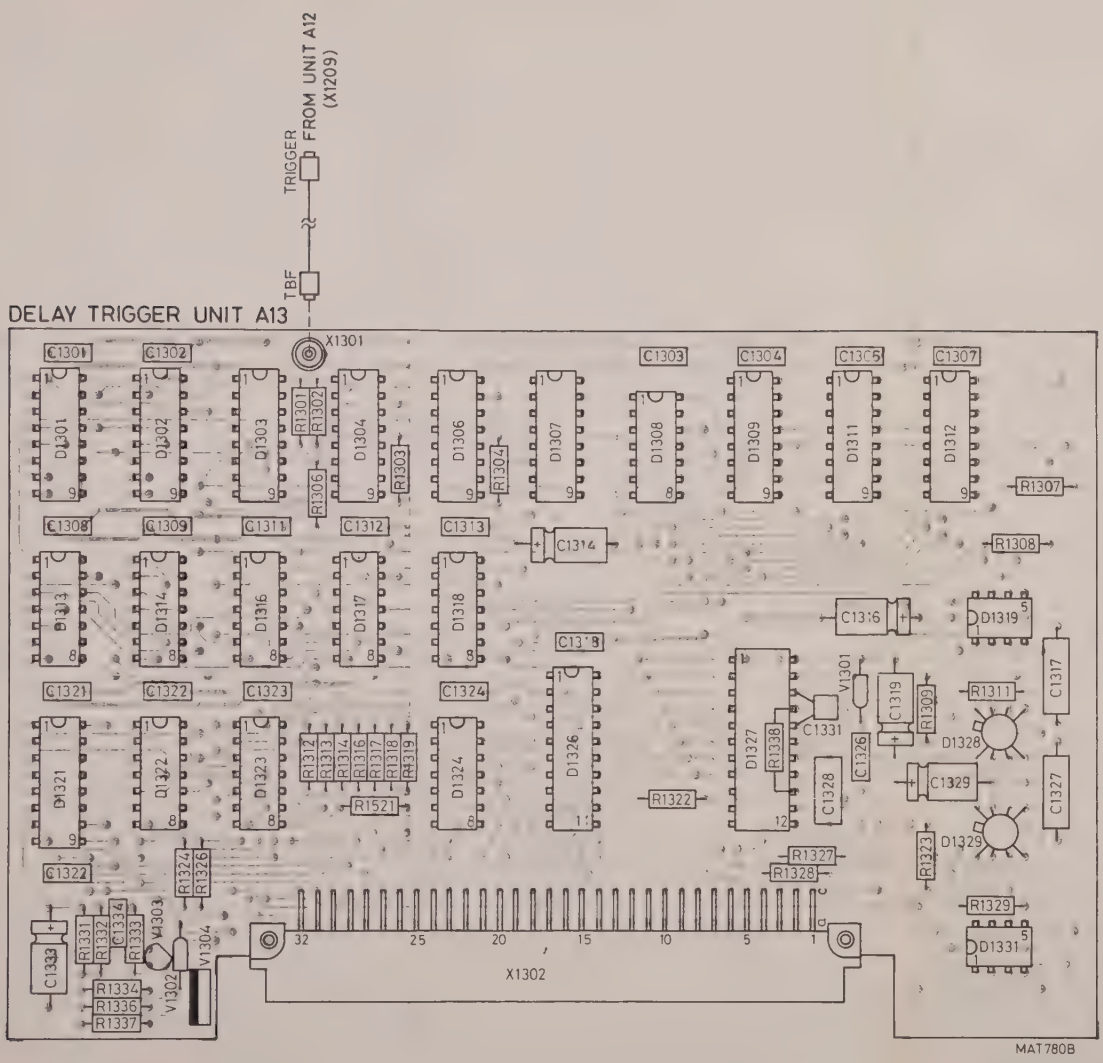

TRIGGER
FROM UNIT A12
(X1209)
TBF
DELAY TRIGGER UNIT A13
X1301
X1302
MAT780B

Fig. 6.2.58.

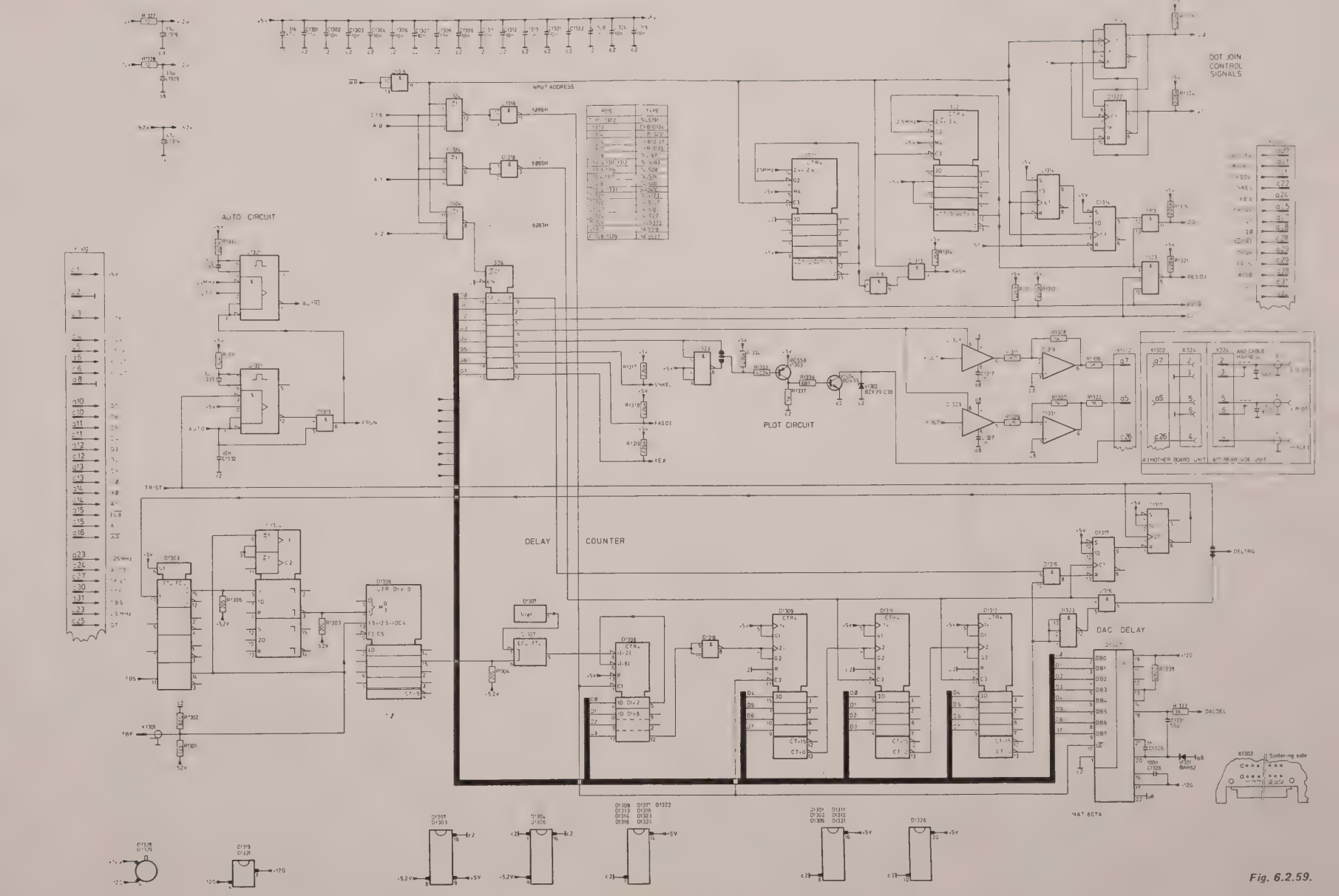

DOT JOIN CONTROL SIGNALS
INPUT ADDRESS
AUTO CIRCUIT
PLOT CIRCUIT
DELAY COUNTER
DAC DELAY
A3 MOTHER BOARD UNIT
A1 REAR SIDE UNIT
A60 CABLE HARNESS
Soldering side
MAT 807A

Fig. 6.2.59.

6.2.14. I.E.C. unit A14

There is a connector X1401 available on the motherboard unit A3 in which no plug-in unit is placed.

Here the I.E.C. bus interface option PM 3325 can be placed.

For mounting instructions refer to the sheet which is delivered with the PM3325.

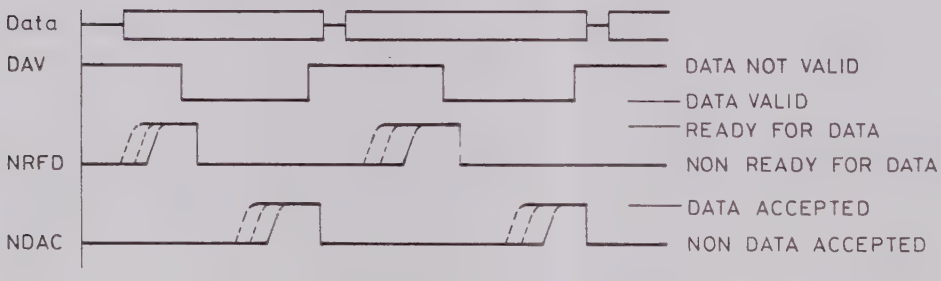
– PM3310C instruments are already provided with an I.E.C. unit A14.
– For service spare parts refer to chapter 12 "PARTS LISTS".

6.2.14.1 General description (refer to block diagram).

An IEC bus line interface is used in multidevice systems to connect the instruments in parallel to the same interface lines. Each instrument has its own specific address (selected with switches in the instrument) so that an instrument is only listening after it has received its specific address, in IEC terms is called **My listen Address (MLA).** The Listen addresses are generated by the controller of the system (e.g. a computer) and are transmitted via the data lines of the bus during an address or interface message the attention line (ATN) is active to indicate that the information on the data lines have a special interface function.
The IEC bus can be split up into three functional parts: the data bus, the handshake bus and the management bus.

- **The Data Bus** is used to transport messages for the device functions as well as for the interface functions and consists of 8 lines **(D101...8).**
- **The Handshake Bus** controls the correct transfer of data bytes with the next three signals.

Data Valid (DAV) indicated the condition of information on the 8 DIO lines.
Not ready for data (NRFD) indicates the condition of readiness of device (s) to accept data.
Not data accepted (NDAC) indicates the condition of acceptance of data by devices.
A timing diagram for the handshake cycle is shown in the figure,take notice that the cycle is as fast as the slowest instrument.



MAT 898

- **The management bus** is used to manage an orderly flow of information **accross** the interface.

Herefore the next five signals are available:
Attention (ATN) specifies how data on the DIO lines are to be interpreted. Active indicates a message is transferred via the data bus (for example a listen address), not active status is present during normal data transfer (for example a command for the oscilloscope).
Interface clear (IFC) places the interface of all interconnected devices in a known quiescent state.
Service Request (SRQ) indicates that one of the instruments wants the attention of the controler for example to give an error message.
Remote enable (REN) sets an instrument to its remote-control mode, if it is in the addressed state.
End of identify (EOI) indicates the end of a multiple byte transfer.

NOTE: Because of the negative logic used for the IEC-bus the signals are "true" (active) when they have a low level, HOWEVER all signals at the lefthand of the buffers D1406-07-16-17 are given for positive logic, so "true" is a high level.

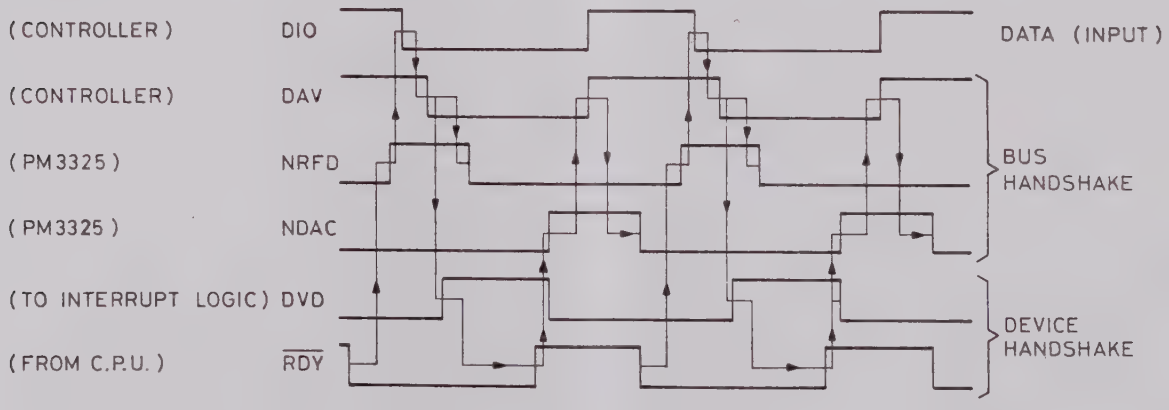
How does the interface function?

Initiation:

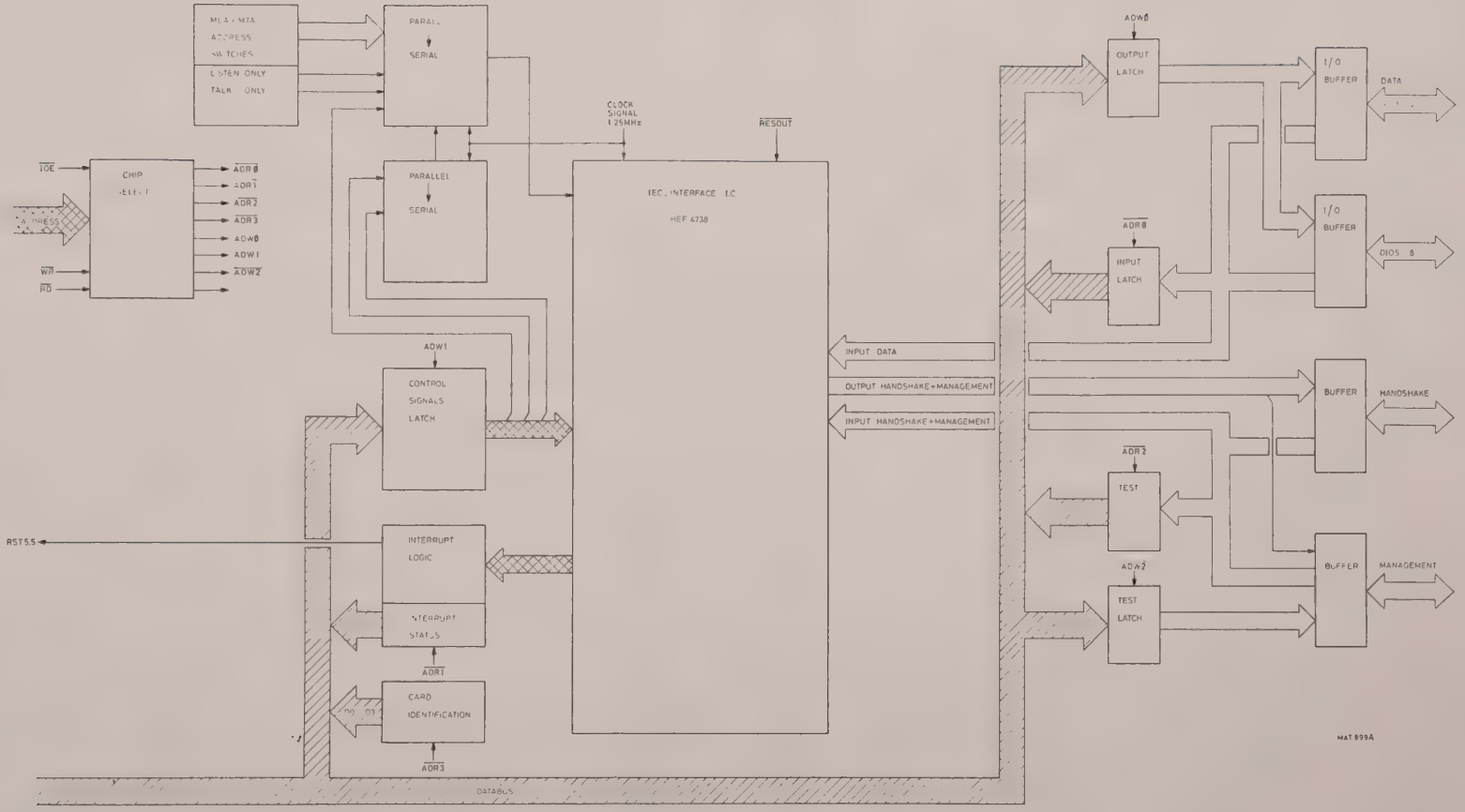
When the oscilloscope is switched-on, the C.P.U. reads the card code to identify which of the optional interfaces has been fitted. In this case it is the PM3325 so the C.P.U. starts with the initiation of the interface by sending control-signals to the latch D1424. The integrated circuit D1408 (HEF 4738) reads the status of the switches for MLA/MTA, TALK ONLY and LISTEN ONLY and some control signals via the two shift registers D1429 and D1431. The listen address is put into a register of D1408.
Now the interface is ready to operate.

Receiving:

First the system-controller sends a listener address via the DIO lines (so ATN is "true"). If the address is equal to the MLA in the HEF4738, the interface becomes the listener status, this action is performed without intervention of the C.P.U. of the oscilloscope. Once in the listener state all succeeding data (without ATN="true") is read by the C.P.U. of the oscilloscope in the following way: The C P U sets via the control signals latch the signal READY FOR NEXT MESSAGE to the active (low) state.
After the falling edge of the RDY signal the HEF 4738 starts with the bus handshake. First Not Ready For Data (NRFD) on connector X1402-pt8 is made high by the PM3325, so the interface is ready to receive data (for remember the IEC-bus uses negative logic). Then the controller puts data on the DIO lines and makes Data Valid (DAV) on connector X1402-pt7 "true" (=low). DAV is received by the HEF 4738 and as a result Data Valid Device (DVD) on pin 17 becomes "true" (=high). When DVD becomes high the data is latched into D1426. DVD is also supplied to the interrupt logic, so the C.P.U. of the oscilloscope interrupts its current program and checks the interrupt status D1423. DVD on pin 2 of D1423 is high, consequently the oscilloscope sets listen enable high, to inhibit interrupts caused by DVD and reads the contents of the input latch D1426. Subsequently the C.P.U. sets the signal ready for next message high and reads DVD, when DVD becomes low the C.P.U. resets the signals ready for next message and listen enable. The latter enables the DVD signal again to interrupt the oscilloscope.



MAT 900

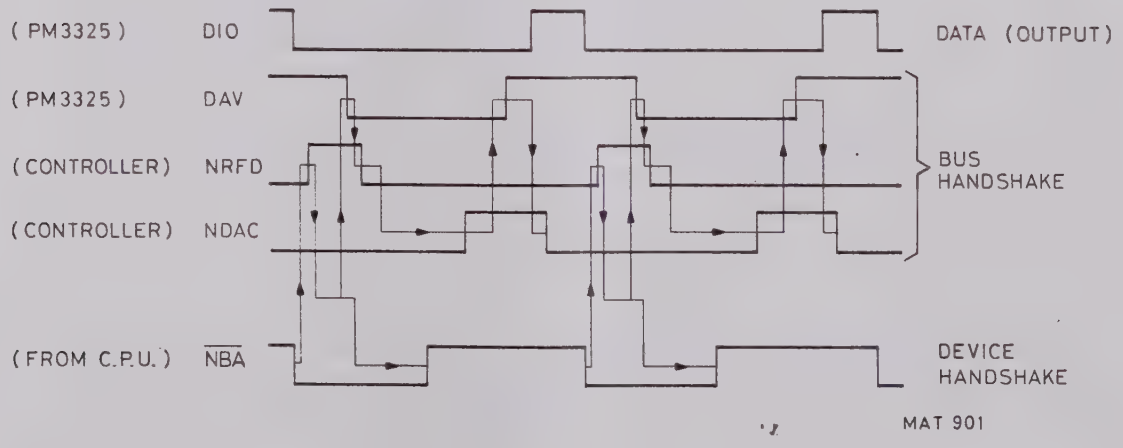

MLA / MTA
ADDRESS
SWITCHES
LISTEN ONLY
TALK ONLY
PARAL.
SERIAL
CLOCK
SIGNAL
1.25MHz
RESOUT
IOE
CHIP
SELECT
ADDRESS
WR
RD
ADR0
ADR1
ADR2
ADR3
ADW0
ADW1
ADW2
PARALLEL
SERIAL
IEC-INTERFACE I.C
HEF 4738
INPUT DATA
OUTPUT HANDSHAKE+MANAGEMENT
INPUT HANDSHAKE+MANAGEMENT
OUTPUT
LATCH
I/O
BUFFER
DATA
DIO5 8
INPUT
LATCH
BUFFER
HANDSHAKE
TEST
BUFFER
MANAGEMENT
TEST
LATCH
CONTROL
SIGNALS
LATCH
RST5.5
INTERRUPT
LOGIC
INTERRUPT
STATUS
CARD
IDENTIFICATION
DATABUS
MAT 899A

Transmitting:

The PM3310 in combination with th PM3325 is capable to send status messages to a controller in case of an error condition. If the oscilloscope has such a message, it asks the attention of the controller by means of the Service Request (SRQ) line on connector X1402-pt11. The SRQ line becomes active after the C.P.U. has set the request for service bit of the control-signals latch D1424. All the connected instruments use the same SRQ line so the controller must check which of the instruments has caused the service request. This is called SERIAL POLLING therefore the controller must address the instruments one by one as talker and read the status-byte: The seventh bit of the status-byte indicates that the corresponding instrument has asked for service, the other bits give the status condition of the instrument.
The status word is built-up as follows:

bit 8	Not used
bit 7... "1"	A SRQ has been given by the PM3310
"0"	No SRQ is given
bit 6 ..."1"	An ALARM is given to indicate that there is a fault condition.
"0"	No ALARM is given
bit 5 ..."1"	The PM3310 is busy with the programmed action
"0"	The PM3310 is ready with the programmed action
bit 4 ..."1"	Data on bus valid } not used for PM3310
'0"	Data on bus not valid } not used for PM3310
bit 3 bit 2 bit 1	Not used

The sequence of signals during an error condition is as follows.
First the C.P.U. activates the request for service signal of integrated circuit D1424 pin 6. The result is an active SRQ signal on connector X1402-pt11. The controller sends talk addresses, once become talker the C.P.U. puts the status-byte in the output latch and activates the signal new byte available (D1424 pin 19). Subsequently the PM3325 waits till NRFD (X1402-pt8) becomes high and then DAV (X1402-pt7) is made active (= low) and NRFD is reset by the controller.
When the controller has received the data, it makes the signal NDAC (X1402-pt9) high, the PM3325 answers with setting the DAV high and then the controller resets the NDAC signal.



6.2.14.2 Chip select

To select chips of the IEC interface board the inputs of the chip select circuit must have the logic levels as given in the next table.

INPUTS					ADDRESS - BUS	OUTPUT	SELECTED FUNCTION	
$\overline{IOE}$	A1	A0	$\overline{RD}$	$\overline{WR}$	HEX. - CODE			
0	0	0	1	0	80E0(H)	ADWØ	Output latch	D1427
0	0	1	1	0	80E1(H)	ADW1	Control signals latch	D1424
0	1	0	1	0	80E2(H)	$\overline{ADW2}$	Test latch	D1413
0	0	0	0	1	80E0(H)	$\overline{ADR0}$	Input latch	D1426
0	0	1	0	1	80E1(H)	$\overline{ADR1}$	Interrupt status	D1423
0	1	0	0	1	80E2(H)	$\overline{ADR2}$	Test latch	D1428
0	1	1	0	1	80E3(H)	$\overline{ADR3}$	Card identification	D1428

6.2.14.3. Card identification

After a reset of the PM3310 or after switching-on the power, the C.P.U. of the oscilloscope checks if an optional interface has been fitted into connector X1402 (of the PM3310). This is performed by putting the hexadecimal code 80E3 on the address bus and reading the card code (0010 is the code of the PM3325) via the data bus.

"0" if an optional interface has been fitted.

6.2.14.4 MLA/MTA address, listen only and talk only.

With switches S1401-2-3-4-5 the listen address as well as the talk address is selected.
S1401 is the least significant bit and S1405 the most significant bit.
Do not use de code 00000 or 11111, the first is generally used as the address of the system controller the latter is the code for the commands "unlisten" and "untalk".
The MLA/MTA code is converted to a serial pattern with integrated circuit D1431 and is shifted into a register of D1408.
"Talk only" is not used if the PM3325 is used in combination with the oscilloscope "Listen only" can be used if another instrument connected to the oscilloscope is not capable to generate addresses, then that instrument must be switched to its "talk only" position.

6.2.14.5 Control-signals latch

Via integrated circuit D1424 the C.P.U. of the oscilloscope can control functions of the IEC-bus interface such as request for service, and the handshake between the interface board and the oscilloscope. The next table gives the signals with a description of the function.

SIGNAL	DESCRIPTION
$\overline{\text{READY FOR NEXT MESSAGE}}$	Indicates the readyness of the C.P.U. to receive the next character.
LISTEN	"0" indicates that the HEF4738 (D1408) may be addressed as talker as well as listener at the same time. "1" causes an unaddressing of the listener function, when a talk address is given and an unaddressing of the talker function, when a listen address is given.
REQUEST FOR SERVICE	The oscilloscope wants the attention of the system controller.
RETURN TO LOCAL	Not used in PM3310.
TEST ENABLE	Not used in PM3310.
END OR IDENTIFY	Not used in PM3310.
LISTEN ENABLE	Signal to enable (if low) or inhibit an interrupt caused by "DATA VALID DEVICE" via D1403 pin 4.
$\overline{\text{NEW BYTE AVAILABLE}}$	An active low signal indicates that the oscilloscope has data to be transmitted.

6.2.14.6 Interrupt logic, interrupt status.

The output signal RST 5,5 of the interrupt logic (D1419 pin 4) gives an interrupt to the microprocessor of the instrument, when the input of flip flop D1419 becomes low. Four signals can cause an interrupt in this way, namely DATA VALID DEVICE, DEVICE CLEAR, LOCAL and TALKER ACTIVE STATE. Flip flop D1419 is reset by the positive going edge of signal $\overline{\text{ADR1}}$ with the circuit consisting of R1402, C1421, D1411, D1412 and D1422. $\overline{\text{ADR1}}$ is generated by the chip select circuit when the interrupt status is read.
By reading the interrupt status the C.P.U. of the oscilloscope can check the status of the interface board after an interrupt has been received. The next table gives a survey of the statussignals with a description.

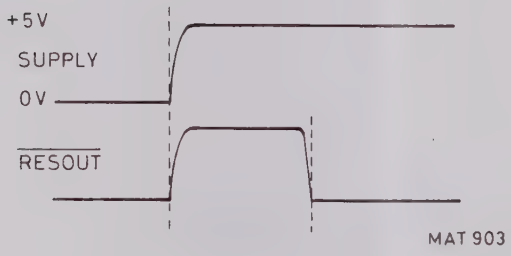
SIGNAL	DESCRIPTION
DATA VALID DEVICE	"1" indicates the IEC-bus interface has received data for the oscilloscope.
DEVICE CLEAR	"1" after the system controller has transmitted the command "device clear" or "selected device clear"
TRIGGER	"1" after the system controller has transmitted the command "device clear"
LOCAL	"1" after the system controller has transmitted the command "device clear"
SERIAL POLL	"1" after the system controller has transmitted the command "serial poll enable". The signal is reset by the command "serial poll disable".
TALKER	"1" indicates that the interface board is in the talker active state
END OR IDENTIFY	"1" after the system controller has transmitted an active EOI.
HANDSHAKE	Becomes "1" when the signal DAV (source transfer state) becomes true. It is reset by the signal $\overline{\text{new byte available}}$.

6.2.14.7 Clock signal, $\overline{\text{RESOUT}}$ signal.

The clock pulse of 1,25 MHz from the PM3310 is used for the internal synchronisation of the HEF4738 (D1408) and for the two 8 bit shift registers (D1431 and D1429).

MAT 902

The $\overline{\text{RESOUT}}$ signal is used to reset the HEF4738 to initial values and to reset the flip-flop's of integrated circuit D. The figure shows the signals when the instrument is switched on.



MAT 903

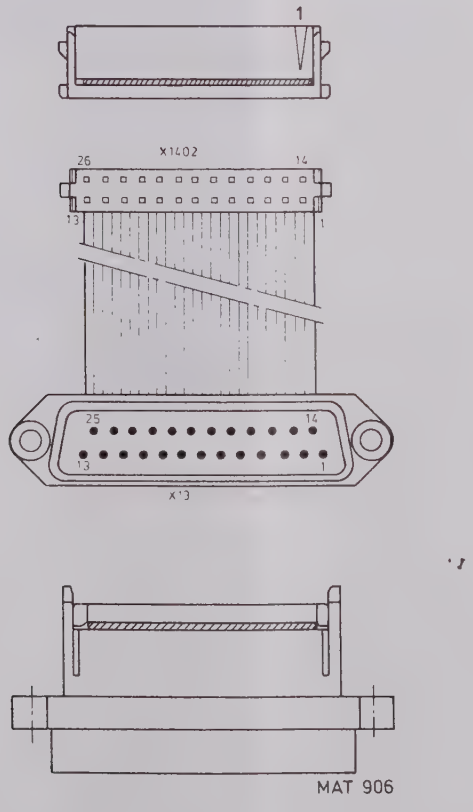
6.2.14.8 Output latch, input latch.

The output data, coming from the C.P.U. of the oscilloscope, are latched into the D-flip flops of the output latch when the signal ADW2 becomes high. The 8-bit output of the latch is continuously connected to the nand-gates in the I/O buffers D1416 and D1417 because the $\overline{\text{enable}}$ input (pin 1 of D1427) has been connected to ground.
The input data, coming from the I/O buffers D1416 and D1417, are latched into the eight D-flip flops of D1426 when the signal "Data Valid Device" (DVD) becomes high. The output of the D-flip flops is connected to the date bus when signal $\overline{\text{ADR0}}$ becomes low, at that moment the input data is read by the C.P.U. of the oscilloscope.

6.2.14.9 I/O buffers.

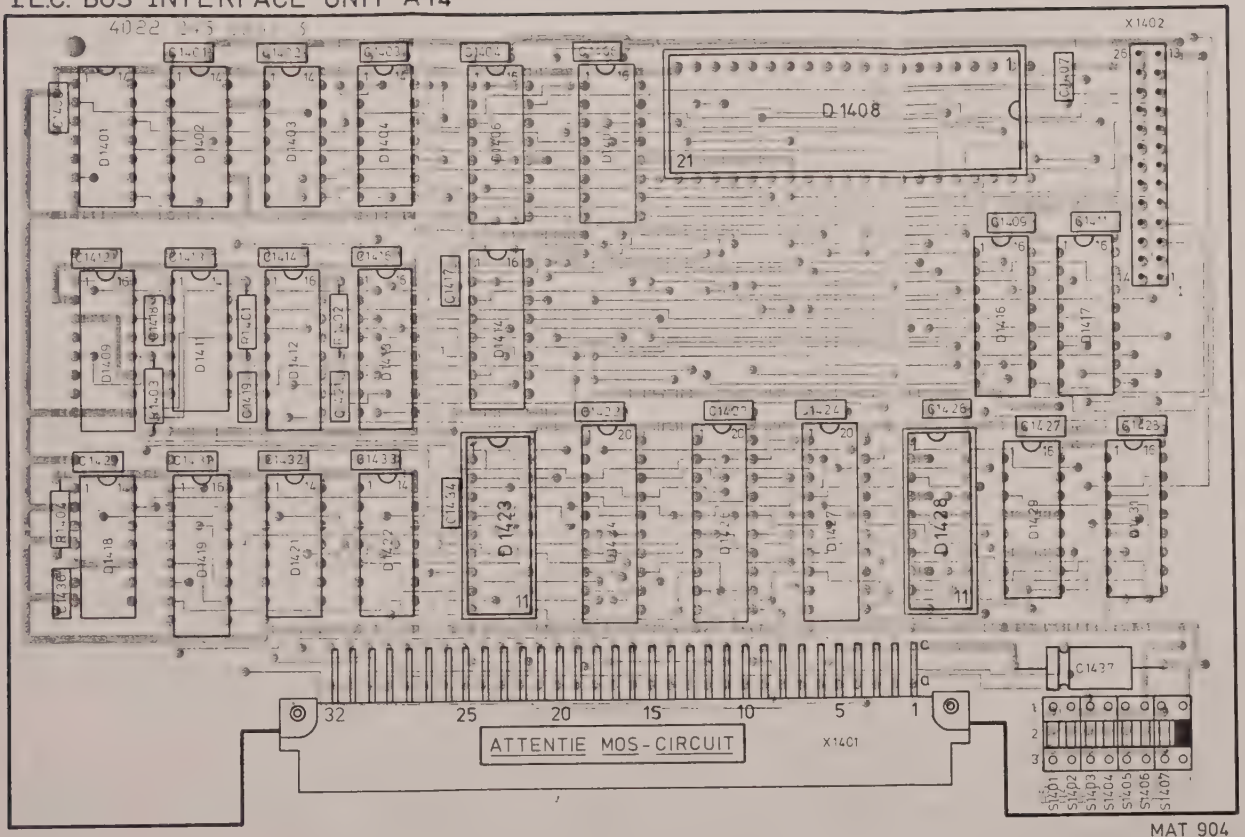
As buffers for the eight DIO lines D1416 and D1417 are used. They consist of inverters, nand gates and resistors. The input data is fed to the input latch and to the HEF4738 (D1408) via the inverters. Output data, coming from the output latch is fed to the nand-gates. The output data is put on the DIO lines when the signal "TALKER ACTIVE STATE" is high. The two remaining buffers (D1406 and D1407) are used for the handshake signals and management signals. Here the enable signals for the nand-gates have been connected to ground so the outputs are always enabled.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A0 ... A1		A4		Address bits from system address bus
	ATN	A14		Attention
D0 ... D7	D0 ...D7	A14	A4	Data bits from system data bus
	DAV	A14		Data available
	D101 ... D108	A14		Data input/output bits
	EOI	A14		End or identify
$\overline{IOE}$		A4		I/O address decoding signal
	NDAC	A14		Not data accepted
	NRFD	A14		Not ready for data
	IFC	A14		Interface clear
$\overline{RD}$		A4		Signal READ from microprocessor
	REN	A14		Remote enable
RESOUT		A4		Microprocessor RESET OUTPUT signal
	RST 5,5	A14	A4	Restart 5,5 signal to microprocessor
	SRQ	A14		Service request
$\overline{WR}$		A4		Signal WRITE from microprocessor
1,25MHz		A12		
+5V		A15		
		A15		

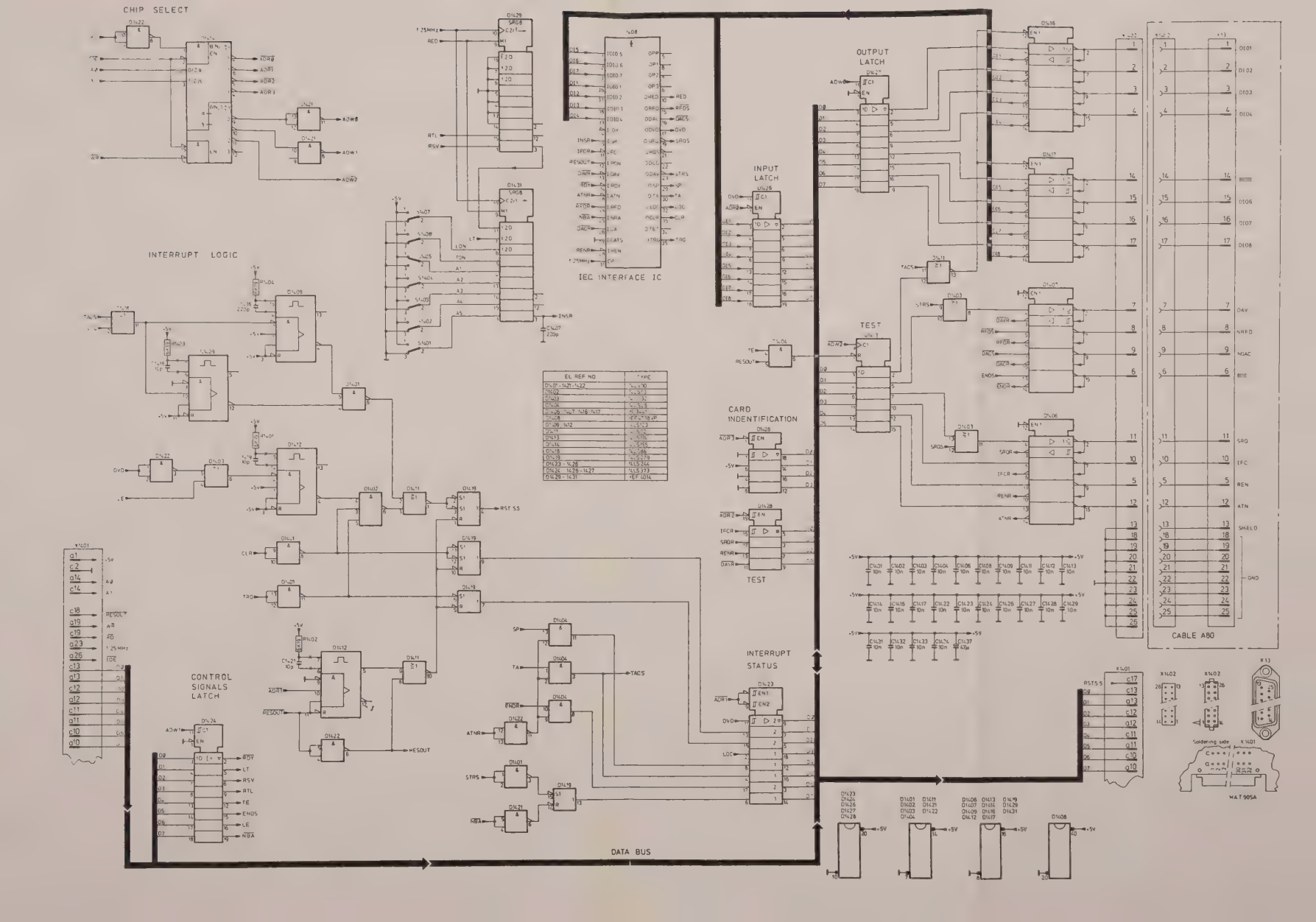


MAT 906

I.E.C. BUS INTERFACE UNIT A14



MAT 904


CHIP SELECT
INTERRUPT LOGIC
CONTROL SIGNALS LATCH
IEC INTERFACE IC
OUTPUT LATCH
INPUT LATCH
TEST
CARD INDENTIFICATION
INTERRUPT STATUS
DATA BUS
CABLE A80
WAT 905A
Soldering side

6.2.15. DC power unit A15

The DC power unit A15 contains the following circuits:

- DC output circuits
- High voltage converter and EHT unit
- Memory back-up circuit
- Protection circuit for the +5 V
- Cathode-ray tube circuit
- Z-amplifier circuit
- Illumination circuit
- Line signal circuit

Each of these circuits is now separately described.

DC output circuits

The voltages on the secondary windings of transformer T1602 on the AC power unit A16 are applied to several rectifiers and voltage doublers.

The bridge rectifiers provide for the +5 V, –5 V, +6 V, –6 V, +12 V, –12 V and +40 V supply voltages. The voltage doublers provide for the +125 V and –125 V supplies.

A –5 A supply voltage is derived from the –12 A via D1501.
A +6,5 V supply is derived from the +12 A by R1561, C1547 and V1544.
A +94 V supply is derived from the +125 V via R1572, C1548 and zener diodes V1554, V1556.

The secondary windings providing the voltages for the various circuits in the oscilloscope are completely isolated from the mains power supply.
Each supply voltage is individually rectified and smoothed.

The filament of the c.r.t. is supplied by the 6.3 V heater voltage between f_1 and f_2.

High-voltage converter and EHT unit

A sine-wave converter formed by transformer T1501 and V1501 converts the +40 V d.c. into 1500 V a.c. with a frequency of approximately 30 kHz.
This voltage is applied to a voltage multiplier on EHT unit A23. The output voltage of this multiplier, 6.5 kV, is applied to g8 of the c.r.t.

Furthermore, the converter output of 1500 V is also rectified and smoothed by V1502, C1502, R1514 and C1503 and applied to the c.r.t. cathode. It is also fed back to the positive input of operational amplifier D1503 to stabilise the cathode voltage of the c.r.t. and thus prevent any variations in c.r.t. sensitivity.

A reference voltage, obtained from divider R1578, R1591 and R1577 is applied to the negative input pin 2 of operational amplifier D1503.
The resulting voltage on pin 6 of D1503 now controls the high-voltage converter via R1526.

Memory back-up circuit

Two 1.5 V batteries can be fitted in the instrument for memory back-up.

When this battery back-up facility is used, the information that was stored in the random-access memories (RAMs) before switch-off (i.e. signal information and switch settings) is saved when the POWER switch is OFF.

The RAM memories are normally supplied by the voltage +5 BATT, which is derived from the +5 V via transistor V1549 when the instrument is switched on. In this case, the batteries are protected by diode V1546. When the POWER switch is OFF, the supply for the RAM memories is obtained from the batteries via V1546.

Protection circuit for the +5 V

This circuit protects the TTL circuits in the instrument from damage caused by an excessively high +5 V supply. When, for some reason, the +5 V supply increases to a value above 6 V approx., this +5 V supply is switched off by thyristor V1551 under the control of SCS V1527.

Cathode-ray tube circuit

In addition to the c.r.t., this circuit includes the intensity, focus, astigmatism, trace rotation and geometry controls.

C.r.t. controls

By means of the front-panel INTENS potentiometer R15, the intensity of the display can be continuously controlled.
Focussing of the trace is only possible by means of the internal FOCUS potentiometer R1506 (coarse control) and R1588 (fine control).

Trace rotation is achieved by the trace rotation coil circuit. The coil is mounted inside a mu-metal screen and provides a magnetic field for rotational control of the entire scan. The degree and direction of rotation is determined by the setting of the TRACE ROTATION front-panel preset R16 (screwdriver-operated).
The slider of R16 is connected to the bases of complementary emitter-followers V1558, V1559. The trace rotation coil current is supplied by these transistors, only one conducting at a time depending on the setting of R16.

OPTIMUM ADJUSTMENT

The ASTIGMATISM control R1587 enables the form of the spot to be adjusted by influencing the voltage on c.r.t. grids G2/G4.

Barrel and pin-cushion distortion are automatically minimised by the signal X-Y GEM connected to G5, G6 and G7. In this way, these screening grids are connected to a potential equivalent to the mean voltage of the deflection plates. The signal X-Y GEM is generated in the final amplifier unit A20.

Z-amplifier circuit

a. Intensity control

The output voltage of amplifier D1502 can be varied by INTENS potentiometer R15, to give variable illumination of the c.r.t. trace.

The Z-amplifier receives an input signal ZIN which originates in the microprocessor unit A4.
When necessary, the trace is blanked by this signal ZIN, which is the final outcome of a number of different blanking situations occurring in this instrument. Signal ZIN is amplified by the stage incorporating transistors V1547 and V1553. Transistor V1553 acts as a constant-current source. At the output of this amplifier the a.c. and d.c. components of the blanking signal are routed along different paths.
The a.c. path is via blocking capacitor C1518 directly to the Wehnelt cylinder of the c.r.t. The d.c. component of the signal is fed to the emitters of V1541 and V1537 via a low-pass T-filter, R1571, C1555 and R1569.

The signal is modulated by a frequency of 156 kHz applied to V1541 via diode V1552. The resulting a.c. voltage on the collector of V1537 has a peak-to-peak value that depends on the output voltage of the low-pass filter.

The a.c. collector voltage of V1537 is applied via a symmetrical emitter-follower V1526, V1533 to a peak detector. This peak detector (C1522, V1517, V1516, R1518 and C1516) rectifies the a.c. voltage. Finally, this rectified voltage is added to the cathode voltage and applied to the Wehnelt cylinder G1.

The signal is split into its a.c. and d.c. components in order to isolate the cathode and Wehnelt cylinder, which stand at −1500 V, from the other circuits.

Adjustment of the black level is achieved by potentiometer R1589 in the emitter circuit of V1537 in the d.c. amplifier.

b. Focussing control

The electron beam is focussed using internal focus potentiometer R1588, which controls the emitter voltage of transistors V1539 and V1536. The signal is modulated by a frequency of 156 kHz applied to V1539 via diode V1552. On the collector of V1536 a signal is produced, the amplitude of which depends on the position of potentiometer R1588 (and R15 INTENS).

The a.c. voltage on the collector of V1536 is applied via symmetrical emitter-follower V1524, V1532, to a peak detector. This peak detector (C1521, V1514, V1513, R1516 and C1514) rectifies the a.c. voltage. Finally, this rectified voltage is added to the voltage set by potentiometer R1506 (part of a voltage divider network across the high-voltage converter output) and then applied to the focussing anode g3 of the c.r.t. In this way, the focus voltage also depends on the position of the INTENS potentiometer, which determines the voltage across the divider network R1502, R1506, R1509. This provides a measure of compensation, so that the focus of the electron beam is automatically adapted when the intensity of the trace is varied.

Illumination circuit

The graticule can be illuminated by the indicator lamps E1 and E2. The intensity can be varied by the front-panel ILLUM potentiometer R14, which controls the base, and hence the collector current of transistor V1561, which flows through the lamps. Note that the illumination circuit is not short-circuit proof.

Line signal circuit

The line signal circuit produces a sine-wave voltage for mains triggering that is derived from the input mains voltage.

Photocoupler D1602 on unit A16, which provides isolation between the mains voltage and the oscilloscope circuits, drives the V1564 circuit into saturation, which means that the square-wave voltage appearing on its collector has the same amplitude value for all mains voltages.

The original sine-wave is re-constructed by means of an integrator network R1553, R1551, R1536 and C1546, C1543, C1541.

This signal, LINE, is applied via V1523 and V1531 to the trigger selector.

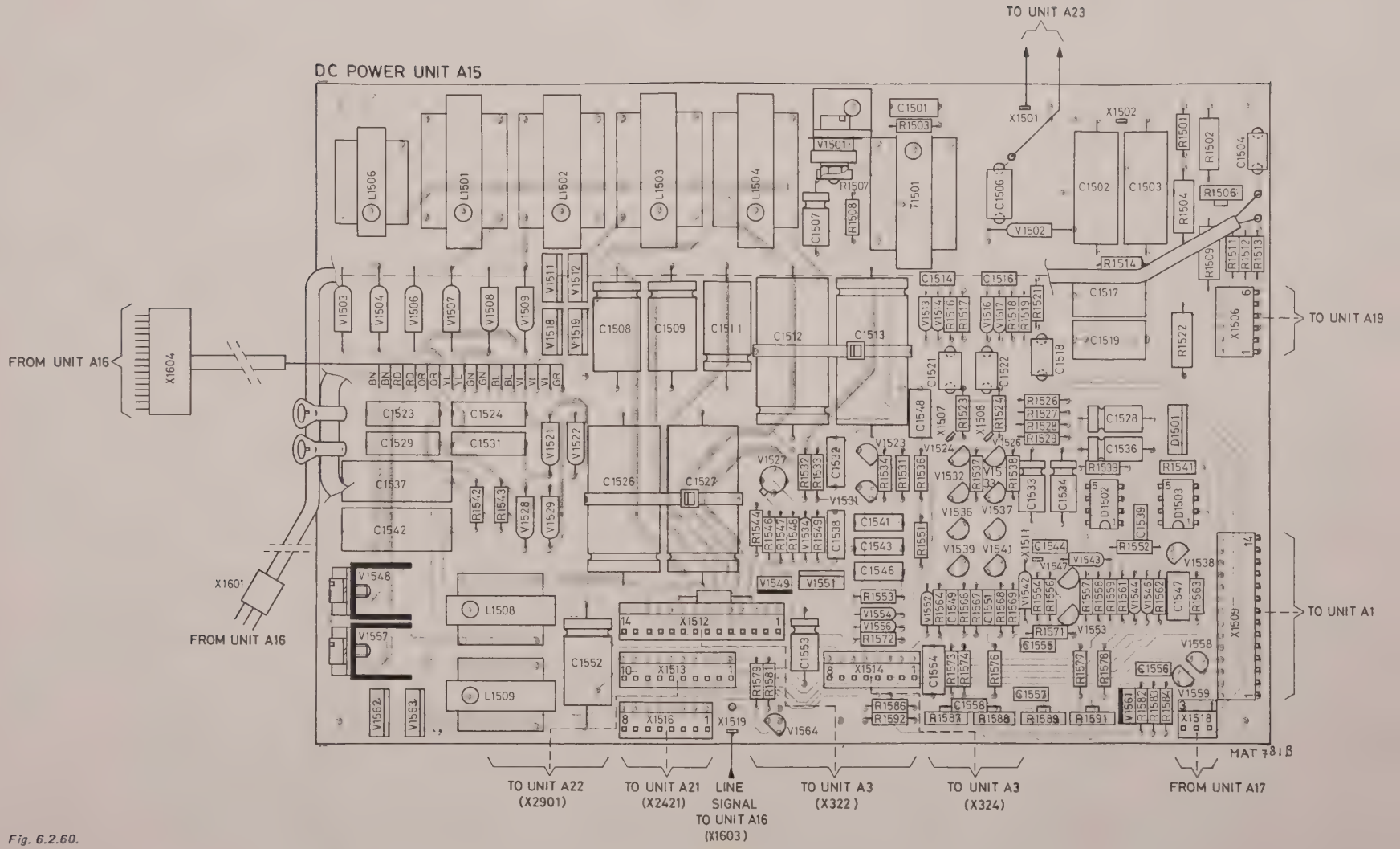

DC POWER UNIT A15
TO UNIT A23
FROM UNIT A16
X1604
X1601
FROM UNIT A16
TO UNIT A19
TO UNIT A1
TO UNIT A22
(X2901)
TO UNIT A21
(X2421)
LINE
SIGNAL
TO UNIT A16
(X1603)
TO UNIT A3
(X322)
TO UNIT A3
(X324)
FROM UNIT A17
MAT 781B

Fig. 6.2.60.

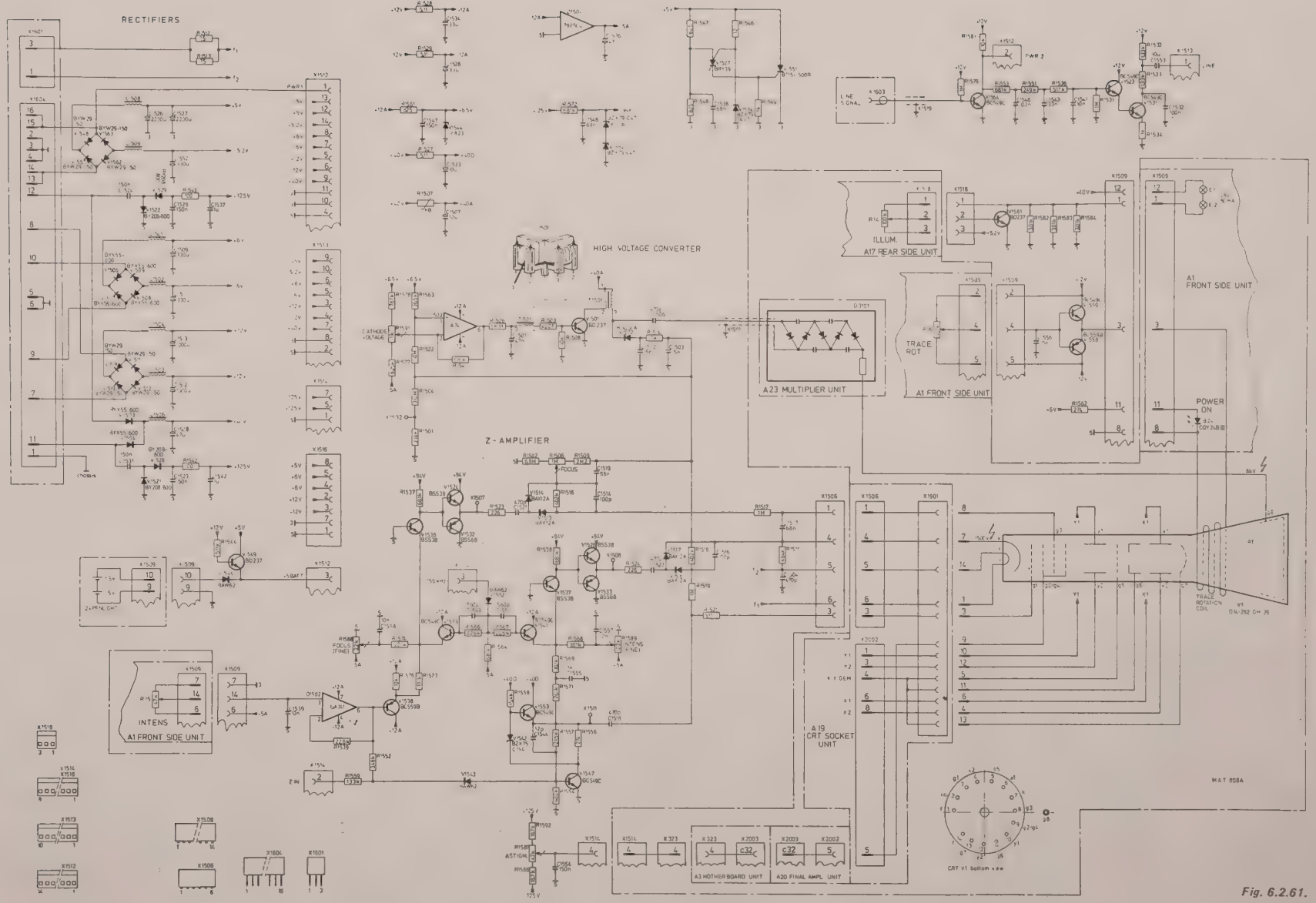

RECTIFIERS
HIGH VOLTAGE CONVERTER
Z-AMPLIFIER
A23 MULTIPLIER UNIT
A17 REAR SIDE UNIT
ILLUM.
A1 FRONT SIDE UNIT
TRACE ROT
POWER ON
INTENS
A19 CRT SOCKET UNIT
A3 MOTHER BOARD UNIT
A20 FINAL AMPL UNIT
CRT VT bottom view
MAT 808A

Fig. 6.2.61.

6.2.16. A.C. power unit A16

The A.C. POWER UNIT comprises a bridge rectifier, a d.c. to a.c. converter regulator and a transformer. Rectifier circuits for the different supply voltages are located on D.C. POWER UNIT A15.

Input circuit

The incoming mains voltage is fed via a double-pole POWER ON/OFF switch S40, fuse F1701 (2 A delayed-action) and mains filter D1701 to the mains rectifier circuit.

This mains rectifier circuit can be matched to one out of two input voltage ranges (115 V or 230 V range) with the MAINS ADAPTER SWITCH S45 on the rear panel of the instrument.

The two-position switching enables the instrument to operate at any mains voltage between 100V and 120V ± 10 % (115 visible in MAINS ADAPTER SWITCH window) and between 220 V and 240 V ± 10 % (230 V visible in window).

Note: The same 2A delayed-action fuse is applicable for both settings of the mains adaptor switch.

The mains voltage is rectified with the diode bridge V1602 and smoothed by capacitors C1606 and C1604, which form a voltage doubler in the 115 V range of S45 and a standard bridge rectifier circuit in the 230 V range of S45.
The voltage across the series circuit of C1606 and C1604 is 250 V to 400 V for both mains voltage ranges.

Switching circuit

The unregulated d.c. voltage is applied in the form of pulses to a resonant circuit consisting of the primary coil of the converter transformer T1602, combined with C1602 and C1603, via switching transistor V1618.
The sine-wave voltage (approx. 800 $V_{p\text{-}p}$) across the primary coil of T1602 is kept constant by regulating the duty cycle of the base current of V1618.
The primary coil of T1601, which is in series with the switching transistor, limits the current through this transistor.
The energy stored in T1601 is fed back to the mains rectifier circuit, during the cut-off time of V1618, via diode V1601.
Diodes V1608 and V1609 eliminate the dissipation through transistor V1618 during the switching period; instead of this, these losses are dissipated in R1604 and R1603.
Diode V1617 improves the base drive for V1618.

Regulator circuit

The regulator circuit consists of integrated circuit D1601 (type TDA 1060), the output (pin 15) of which supplies a square-wave current with a variable duty-cycle to the base of transistor V1616. The signal on the collector of this transistor is applied to switching transistor V1618 via transformer T1603.
The regulator circuit is controlled by the following:

- Feedback voltage (pin 3)
  This is the regulator control voltage derived from the rectifier circuit in the feedback winding of T1602. The value of this control voltage depends on the setting of R1646.

- Feed-forward voltage (pin 16)
  This voltage is derived from the mains voltage and provides direct compensation for mains variation.

- Overvoltage protection (pin 13)
  A voltage is also derived from the mains voltage, via zener diode V1613, to inhibit the regulator output at excessive mains voltages (the level on pin 13 is 600 mV).

- Current limiting (pin 11)
  The voltage drop across the current-sense resistor R1627 controls the regulator circuit in the event of overload.

– Frequency adjustment (pin 7)
  The value of resistance between pin 7 and earth determines the converter frequency. Preset R1647 should be adjusted for a frequency of 20 kHz approximately, i.e. the resonant frequency of C1602, C1603 and the primary coil of T1602.

During normal working, the power supply for the regulator circuit is provided by the rectifier connected to the feedback winding of T1602. Transistor V1622 then conducts, therefore V1621 does not give any current output.

Switching-on and switch-on protection

At the moment of switching-on the instrument, no supply voltages are immediately available in the regulator circuit from T1602. Transistor V1622 is not yet conducting, therefore transistor V1621 is fully conducting and the regulator derives its current via R1616 and R1631. As soon as the converter circuit is working, transistor V1622 conducts and V1621 blocks.

In the event of the instrument giving no converter voltage at switch-on (due to a possible defect), the PTC resistor R1631 warms up and so reduces the current through transistor V1621 to a safe level.

Output circuits

Various supply voltages are derived from the secondary windings of transformer T1602. These supplies are generated on D.C. POWER UNIT A15.

Photocoupler circuit

To enable triggering on a mains signal, this circuit produces a signal derived from the mains voltage. Photocoupler D1602 provides isolation between the mains voltage and the oscilloscope circuits to produce a safe triggering signal. This output signal is applied to transistor V1564 on unit A15, which is driven into saturation to give a square-wave voltage on its collector. This square-wave has a constant amplitude for all mains voltages.

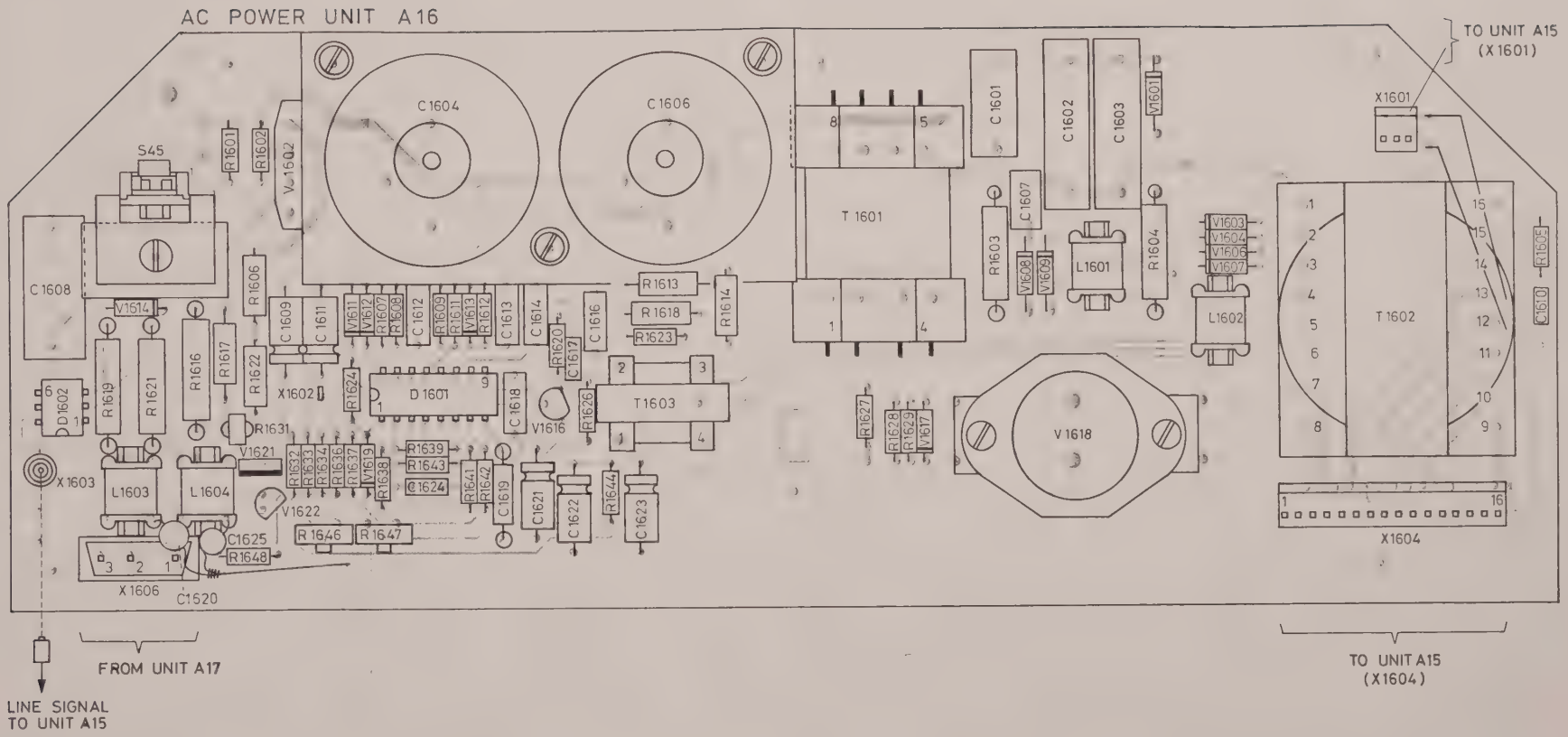
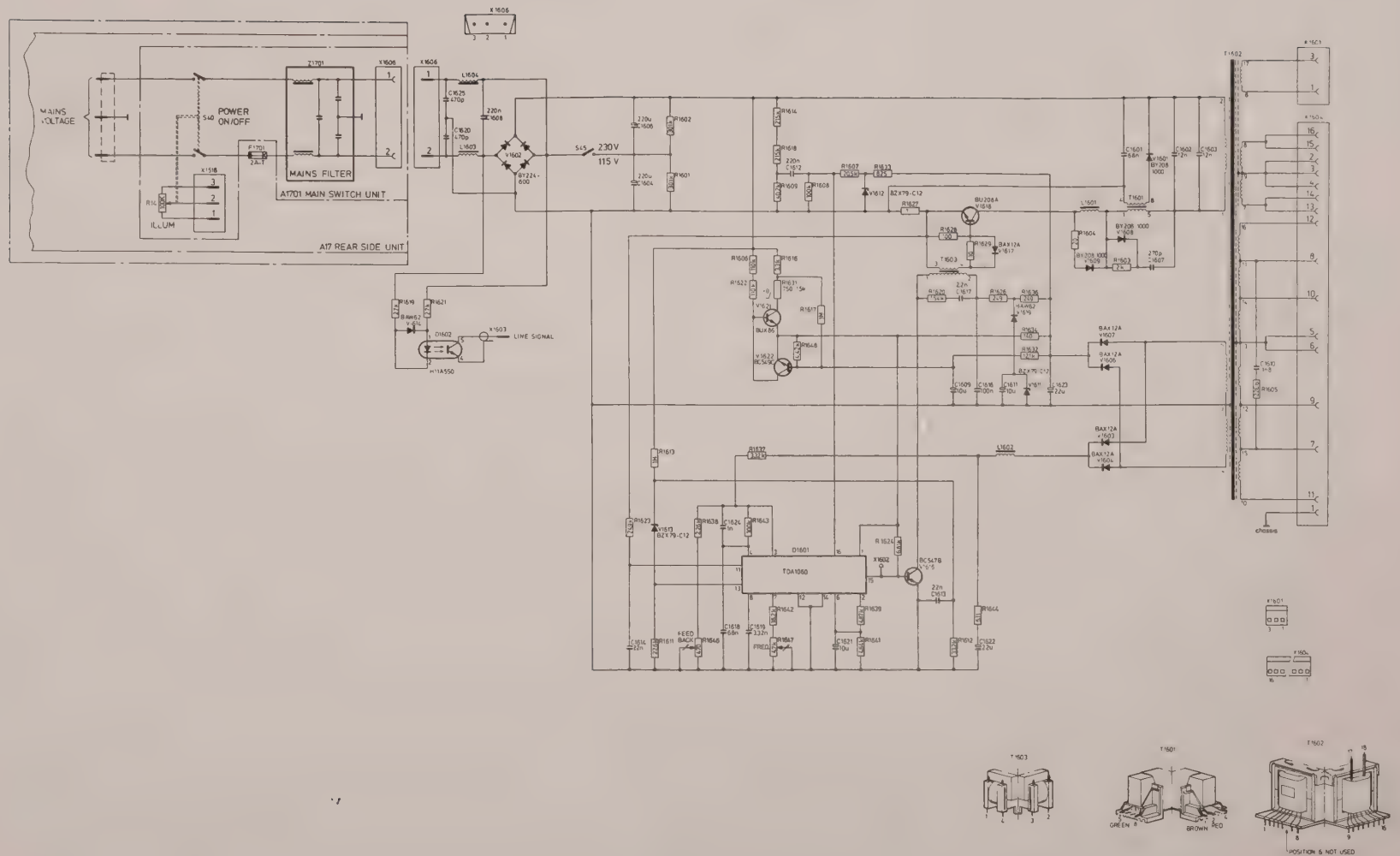

AC POWER UNIT A16
TO UNIT A15
(X1601)
X1601
C1604
C1606
C1601
C1602
C1603
V1601
S45
R1601
R1602
V1602
T1601
C1607
R1603
V1608
V1609
L1601
R1604
V1603
V1604
V1606
V1607
L1602
T1602
R1605
C1610
C1608
V1614
R1606
C1609
C1611
V1611
V1612
R1607
R1608
C1612
R1609
R1611
V1613
R1612
C1613
C1614
R1620
C1617
C1616
R1613
R1618
R1623
R1614
R1619
R1621
R1616
R1617
R1622
X1602
R1624
D1601
C1618
V1616
R1626
T1603
D1602
R1631
V1621
R1632
R1633
R1634
R1636
R1637
V1619
R1638
R1639
R1643
C1624
R1641
R1642
C1619
C1621
C1622
R1644
C1623
R1627
R1628
R1629
V1617
V1618
X1603
L1603
L1604
V1622
C1625
R1648
R1646
R1647
X1606
C1620
X1604
FROM UNIT A17
LINE SIGNAL
TO UNIT A15
TO UNIT A15
(X1604)

Fig. 6.2.62.



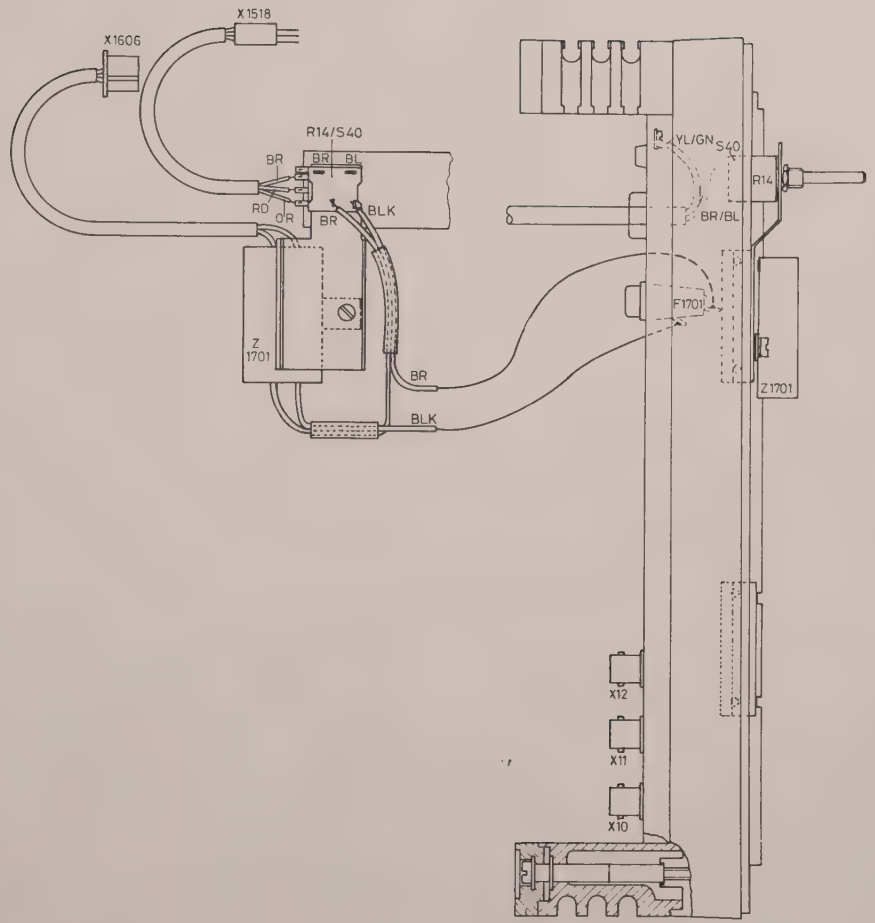
MAT 859A

Fig. 6.2.63.

6.2.17. Rear side unit A17

The rear side unit consists of an aluminium rear cast on which the following items are mounted.

- ILLUM. control R14 - ON/OFF switch S40
- Mains filter Z1701
- BNC output sockets X10-X11-X12 for PLOT output signals
- Fuseholder F1701 and fuse.



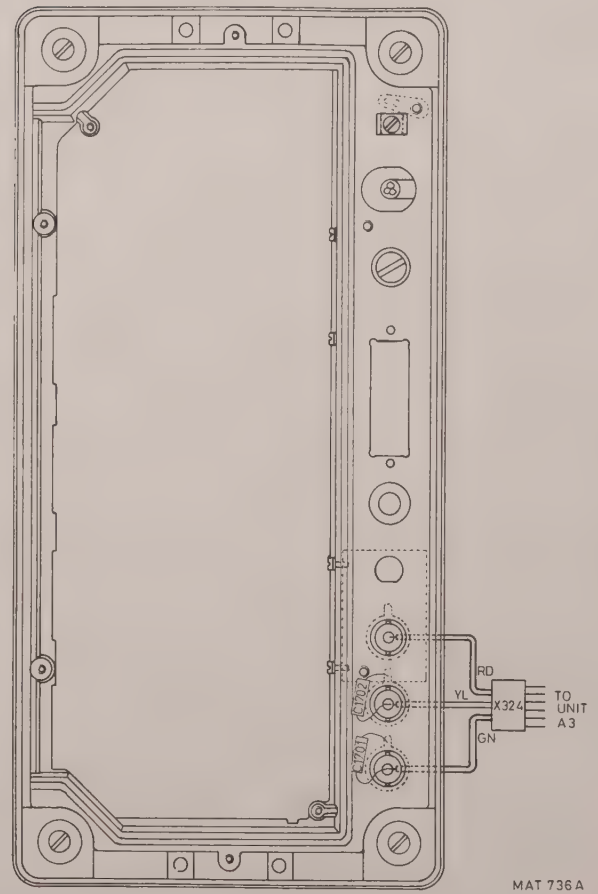


Fig. 6.2.64.

6.2.18. Delay line unit A18

Unit A18 is the delay line unit, which is mounted in the instrument under the C.R.T.

The unit is electrically connected between the channel switch and the delay line compensation amplifier on unit A21.

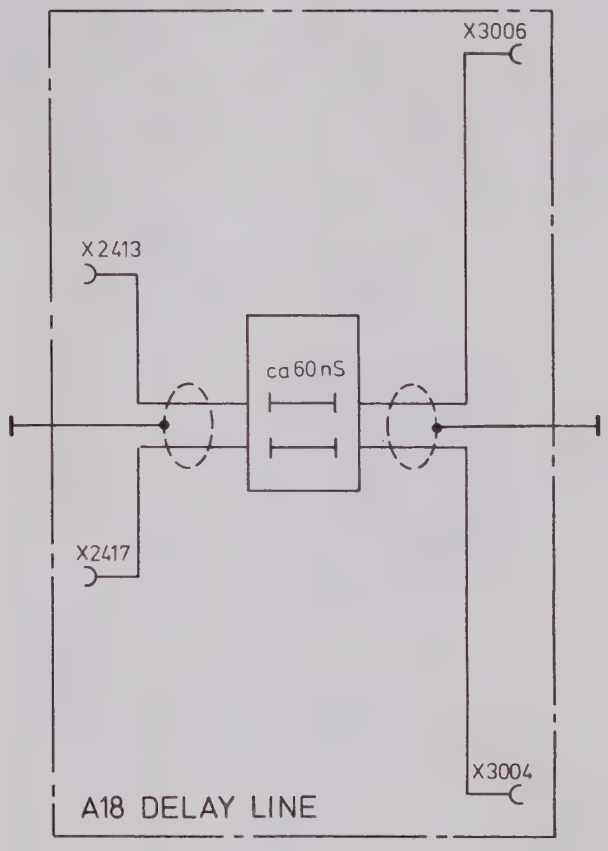


Fig. 6.2.65.

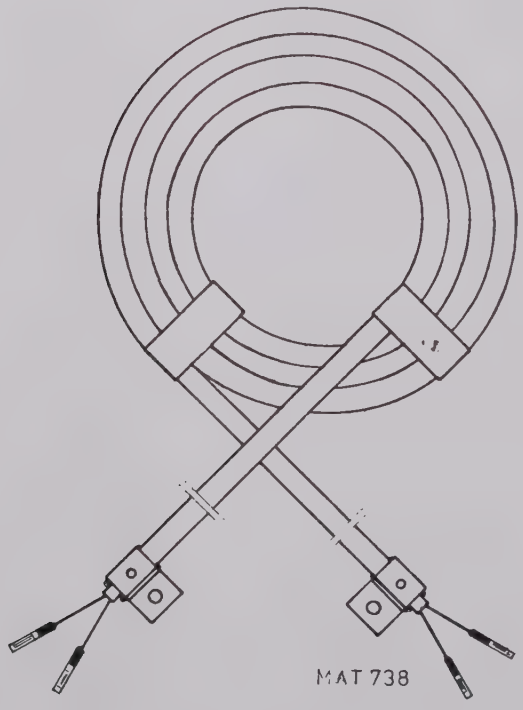


Fig. 6.2.66.

6.2.19. C.R.T. socket A19

The C.R.T. socket unit A19 consists of the socket itself (X1901) and two cables with the connectors X1506 and X2002.

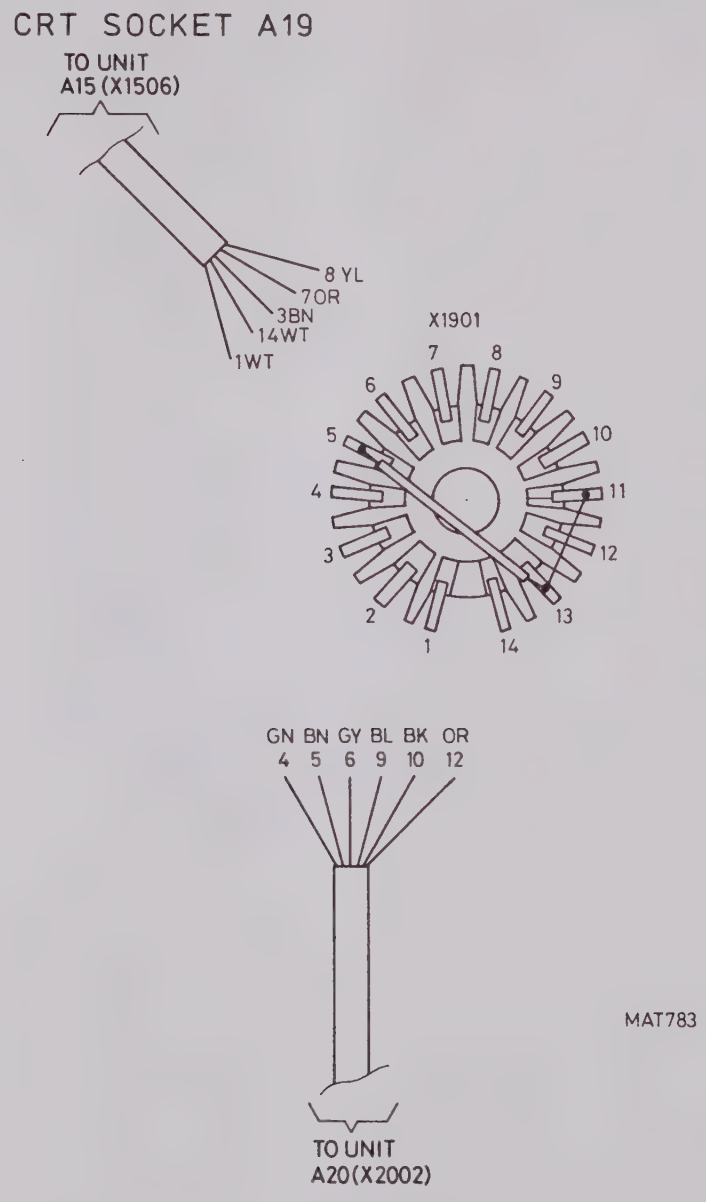


Fig. 6.2.67.

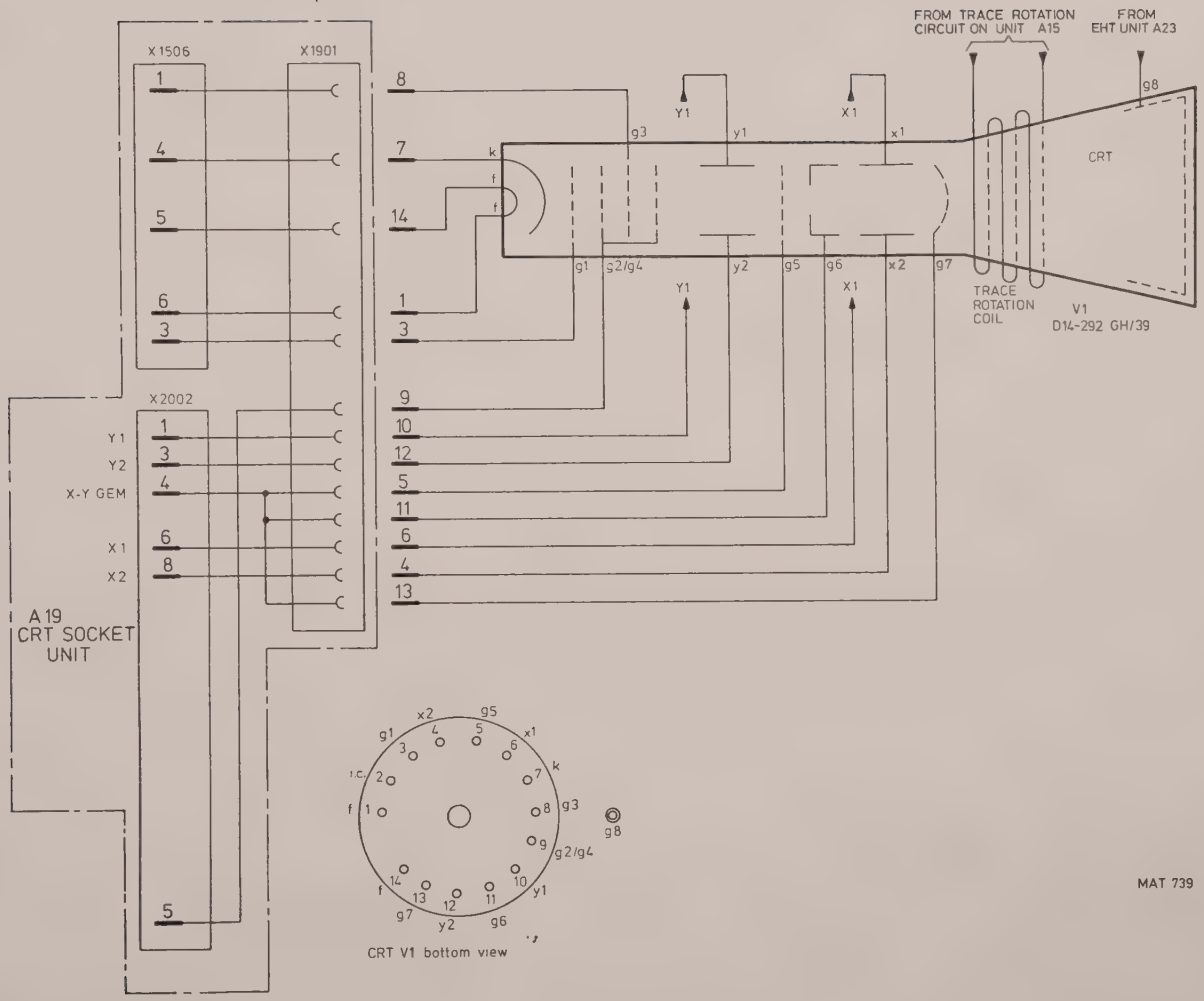

FROM TRACE ROTATION CIRCUIT ON UNIT A15
FROM EHT UNIT A23
X1506
X1901
X2002
A19 CRT SOCKET UNIT
Y1
Y2
X-Y GEM
X1
X2
CRT
TRACE ROTATION COIL
V1 D14-292 GH/39
g1
g2/g4
g3
g5
g6
g7
g8
x1
x2
y1
y2
k
f
CRT V1 bottom view
MAT 739

Fig. 6.2.68.

6.2.20. Final amplifier unit A20

The final amplifier unit consists of the following sections:

- Dot-join system
- Position control system
- Final X and Y amplifiers

6.2.20.1. The Dot-join system

The dot-join system provides the facility for interconnecting the dots on the c.r.t. display to enable a continuous line to be traced. This means that a sawtooth voltage has to be applied to the final amplifier between the dots. The amplitude between adjacent dots in the Y direction controls the amplitude of the sawtooth generator (D2004 and associated components).

Four different signal modes are possible at the input of the dot-join system YDAC:

1. $A_0\ A_1\ A_2\ A_3\ A_4$ ..... A_n
2. $B_0\ B_1\ B_2\ B_3\ B_4$ ..... B_n
3. $A_0B_0\ A_1B_1\ A_2B_2$ ..... A_nB_n
4. $B_0A_0\ B_1A_1\ B_2A_2$ ..... B_nA_n

In these modes, the voltages to be applied to the current source of the sawtooth generator are:

1. $A_1\text{-}A_0; A_2\text{-}A_1; A_3\text{-}A_2; A_4\text{-}A_3; A_n\text{-}A_{(n-1)}$
2. $B_1\text{-}B_0; B_2\text{-}B_1; B_3\text{-}B_2; B_4\text{-}B_3; B_n\text{-}B_{(n-1)}$
3. $A_1\text{-}A_0; B_1\text{-}B_0; A_2\text{-}A_1; B_2\text{-}B_1;$ ..... $A_n\text{-}A_{(n-1)}; B_n\text{-}B_{(n-1)}$
4. $B_1\text{-}B_0; A_1\text{-}A_0; B_2\text{-}B_1; A_2\text{-}A_1;$ ..... $B_n\text{-}B_{(n-1)}; A_n\text{-}A_{(n-1)}$

Circuit D2007 serves to subtract the signals that are derived from multiplexer D2011 via buffers D2009.
In order to obtain the correct signals at the outputs of D2011, multiplexers D2017 and D2018 together with three sample-and-hold gates, in combination with buffers, are introduced.

The sample-and-hold gates are controlled by the TRSH signal (trigger sample hold) which is applied to input 3 of D2018. Depending on the signals Q_0 and Q_1, one of the sample-and-hold circuits D2019, D2026 or D2024 follows the YDAC signal while the other two are holding the information of the last sample, and the sample before it. By means of the Q_0 and Q_1 pulses, the system is scanning the YDAC signal so an analog-shift register is formed.

Signals Q_0 and Q_1 are generated on the delay trigger unit A13. These signals are derived from the write signal $\overline{WR}$ generated by the microprocessor.
Multiplexer D2011 switches the correct signals to the subtract circuit D2007 via the buffer amplifiers D2009. The correct signals are:

- in single channel mode; every time the mean amplitude of two sequential samples is switched to the subtractor
- in dual-channel-mode; two sequential samples of channel A and the two sequential samples of channel B.

(see timing diagram)

The multiplexer D2006 serves to discharge the sawtooth capacitor C2007 and in the case of the 'DOTS' mode, this capacitor is short-circuited so that separate dots are displayed on the screen.
The output of the sawtooth generator is applied to the summing point at the input 2 of D2004. At input 3 of D2004 a crosstalk suppression voltage is present, derived from the multiplexer D2017-3.

For the X channel, the dot-join system functions as follows:

The XDAC signal is applied to input 2 of amplifier D2021. A sawtooth voltage is also applied to that input. The ramp of this voltage is determined by signal SINGLE, which switches multiplexer D2013 so that in single channel operation capacitors C2027 and C2014 are connected in parallel; in dual-channel operation, only C2014 is switched into circuit. The duration of the ramp is determined by the signal RESDJ, which switches multiplexer D2013 so that the capacitor(s) will be discharged.

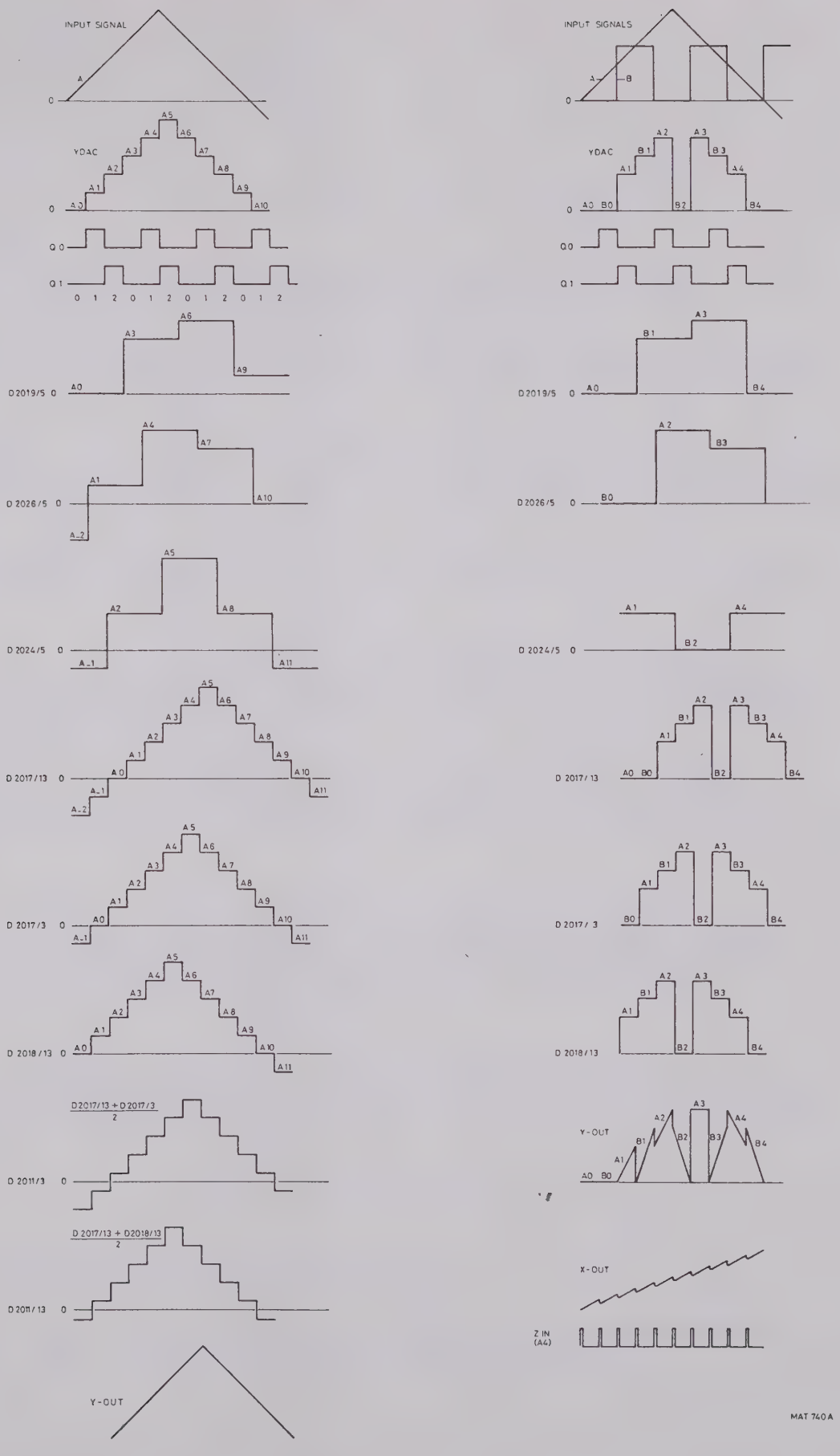

INPUT SIGNAL
A
0
YDAC
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
Q 0
Q 1
0 1 2 0 1 2 0 1 2 0 1 2
D 2019/5
D 2026/5
D 2024/5
D 2017/13
D 2017/3
D 2018/13
D2017/13 + D2017/3
2
D 2011/3
D 2017/13 + D2018/13
2
D 2011/13
Y-OUT
INPUT SIGNALS
A
B
YDAC
A0 B0 A1 B1 A2 B2 A3 B3 A4 B4
Q 0
Q 1
D 2019/5
D 2026/5
D 2024/5
D 2017/13
D 2017/3
D 2018/13
Y-OUT
X-OUT
Z IN
(A4)
MAT 740 A

Fig. 6.2.69.

At pin 3 of D2023 the X OUT signal is available.
This signal may be:
– with no DOT-JOIN facility, a staircase voltage.
– with DOT-JOIN facility, a staircase voltage with a sawtooth voltage on every stair.

6.2.20.2. Y-Position Control System

In the two modes Yx1 and Yx5, a different method of position control is employed for each.

Yx1 mode

In this mode, two different voltages are added to the signal at the summing point (D2001-2):
– A preset voltage for position determination of the displayed memories on the c.r.t. screen.
– An adjustable voltage to position the displayed memories on the screen.

The preset voltage is selected by multiplexer D2012 output 13 and applied to the summing point via D2008 and buffer amplifier D2002 (5.6.7).

The selection of the corresponding memory is controlled by the $\overline{\text{OER}}\emptyset$ ... $\overline{\text{OER2}}$ signals generated on RAM unit A6.
The adjustable voltage is selected by multiplexer D2012 output 3 and applied to the summing point via buffer amplifier D2002 (1,2,3).

The Y*OUT signal is applied via D2008 output 12 and R2036 to the summing point if YEX is 0, as is the case in the Yx1 mode.

Yx5 mode

The preset voltage must not be added in the Yx5 mode, since the base-line of all displayed memories is now situated on the centre-line of the c.r.t. screen (Y POS controls at mid-range position). Multiplexer D2008 is switched by signal YEX = 1 so that the output on pin 15 is connected to earth. This means that no additional voltage is applied to the summing point.

Moreover, the Y*OUT signal is applied to the summing point via resistors R2027 and R2023 in series. The value of these resistors is only one-fifth of R2036, so a 5 times magnified signal is applied to the summing point.

6.2.20.3. Final Y Amplifier

The output of the summing amplifier D2001 (2,3,6) is applied to the differential amplifier V2001 and V2021. The constant emitter current is derived from the current source V2028 and its associated components. Variation in the collector current results in a control voltage for V2006 and V2013, which produces output signals Y2 and Y1 to drive the c.r.t. deflection plates.

6.2.20.4. Final X Amplifier

To obtain the possibility of magnification in the X direction, integrated circuit D2023 is used. This circuit comprises a Darlington pair input stage to obtain a symmetrical signal; a buffer stage and a continuous gain adjustment facility for X magnnification and for X gain.

The final stage functions in a similar way to that of the final Y stage.

6.2.20.5. CAL circuit

The lower part of multiplexer D2008 is controlled by a frequency of 2.5 kHz, derived from the microprocessor crystal frequency of 5 MHz by dividers on the time-base unit.

Input 3 of D2003 is switched between pins 3 and 5 of D2008, i.e. between 1 V and 0 V. Amplifier D2003 serves as a follower circuit with an output of 3 V, adjustable by means of R2017.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
ASTIGM	ASTIGM	A15	A20	Astigmatism
AVSB		A13		Logic 0 in X = A/Y = B mode
DJ		A13		Dot join signal
ENKEL		A13		Single channel mode
OERØ		A6		Output enable RAMØ
OER1		A6		Output enable RAM1
OER2		A6		Output enable RAM2
POSØ		A202		Slider of ACCU position control
POS1		A202		Slider of STO1 position control
POS2		A202		Slider of STO2 position control
POS3		A202		Slider of STO3 position control
QØ		A13		Control signal for dot join
Q1		A13		Control signal for dot join
RESDJ		A13		Reset dot join
TRSH		A13		Trigger for dot join sample and hold
	X1	A20	A19	Horizontal deflection signal
	X2	A20	A19	Horizontal deflection signal
XDAC		A6		Horizontal DAC output signal
XMAGN		A202		Slider of X MAGN control
	XOUT	A20	A13	Horizontal output signal
XPOS		A202		Slider of X POSITION control
	X-Y GEM	A20	A19	Geometry control signal
	Y1	A20	A19	Vertical deflection signal
	Y2	A20	A19	Vertical deflection signal
YDAC		A6		Vertical DAC output signal
YEX		A13		Y-expand
	YOUT	A20	A13	Vertical output signal
ZDJ		A13		Z dot join
2.5 kHz		A12		
+5 V		A15		
+6 V		A15		
−6 V		A15		
+12 V		A15		
−12 V		A15		
+40 V		A15		
+135 V		A15		
−135 V		A15		
⏚		A15		

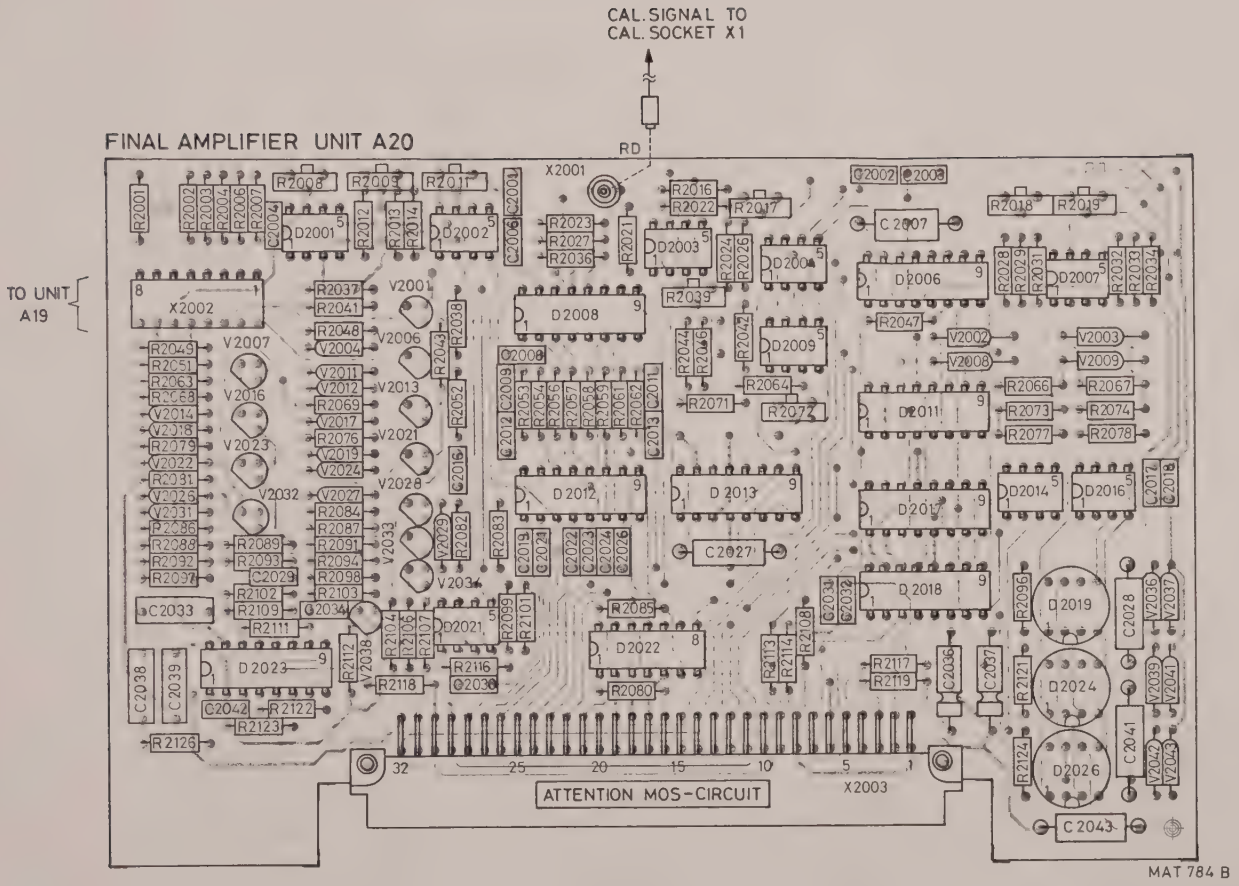

CAL. SIGNAL TO
CAL. SOCKET X1
RD
FINAL AMPLIFIER UNIT A20
TO UNIT
A19
X2001
X2002
X2003
D2001
D2002
D2003
D2004
D2006
D2007
D2008
D2009
D2011
D2012
D2013
D2014
D2016
D2017
D2018
D2019
D2021
D2022
D2023
D2024
D2026
C 2007
C2033
C2038
C2039
C2041
C 2043
V2001
V2006
V2007
V2011
V2013
V2016
V2021
V2023
V2028
V2032
ATTENTION MOS-CIRCUIT
MAT 784 B

Fig. 6.2.70.

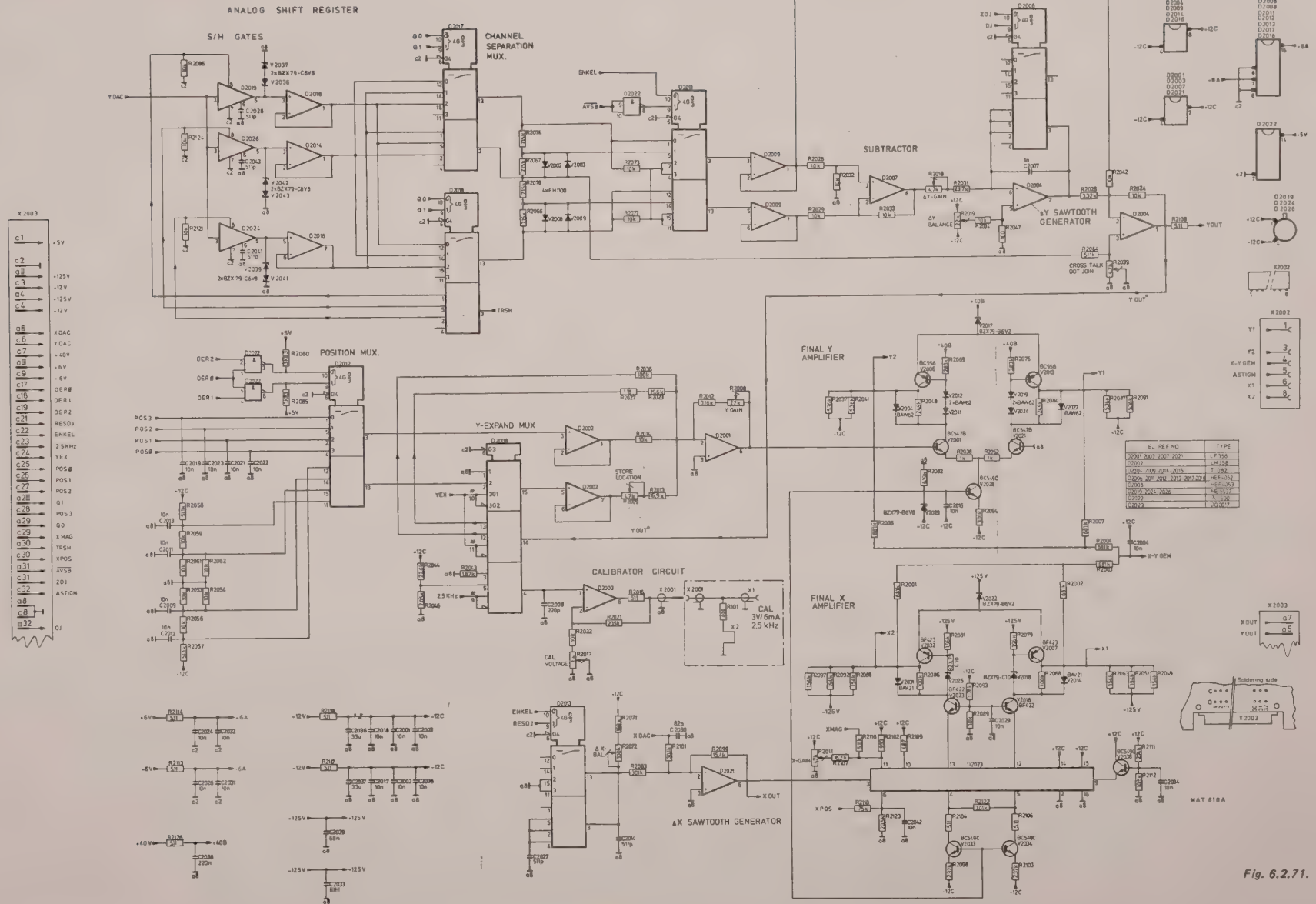

ANALOG SHIFT REGISTER
S/H GATES
CHANNEL SEPARATION MUX.
SUBTRACTOR
ΔY SAWTOOTH GENERATOR
CROSS TALK DOT JOIN
POSITION MUX.
Y-EXPAND MUX
STORE LOCATION
CALIBRATOR CIRCUIT
CAL 3V/6mA 2,5 kHz
FINAL Y AMPLIFIER
FINAL X AMPLIFIER
ΔX SAWTOOTH GENERATOR
MAT 810A
Soldering side

Fig. 6.2.71.

6.2.21. Input amplifier unit A21

6.2.21.1. General

The input amplifier unit is sub-divided into the following sections, as shown in the block diagram.
- Input attenuator
- Amplifier
- Channel switch and mode switch
- Delay line compensation/Track & Hold gate
- Logic circuits (control interfaces)

Briefly, the channel input attenuator reduces the input signal according to the front-panel switch settings or remote signals, and converts it from high to low impedance.
The asymmetrical output signal is applied to the amplifier section to give a symmetrical output, an amplified trigger pick-off and an offset facility. A buffer stage provides for signal inversion and offset before feeding the channel and mode switch section. Here the logic control signals are used to switch the appropriate channels and display modes to the ADC in the storage section of the oscilloscope.

6.2.21.2. Input attenuator

The input stage comprises two identical attenuator circuits. For convenience, only the channel A attenuator is described.

The input signal can be either a.c. or d.c. coupled (via C2476 or K2412) to the attenuators.

Basically, the input attenuator comprises a triple high-ohmic voltage divider and an impedance converter in conjunction with a drift correction circuit. The impedance converter (V2451, V2448) provides a zero level output, adjusted by potentiometer R2643, which feeds a low-ohmic attenuator.

Overall, the attenuation of the input stage is determined by the combination of the selected sections of the two attenuators, according to the setting of the front-panel AMPL/DIV switch. The control sequence is as follows:

The position of the AMPL/DIV switch, the AC/DC switch and the '0' switch are decoded and applied to the reed relays and FET switches (D2411) via the microprocessor system. The reed relays and the FET switches determine the position of the attenuators and are controlled from two 8-bit output ports (D2424, D2426) in the logic circuit. These output ports are controlled via the data-bus and can also be controlled by the IEC-bus interface for remote operation.

The three sections of the high-ohmic voltage divider have an attenuation factor of 1.25, 12,5 and 125 times.

If the front-panel pushbutton '0' is depressed, reed switch K2411 closes and all other reed switches are open. Control for this action is via the output ports of the microprocessor system. With K2411 closed, the input signal is not connected to the attenuator and the impedance converter, via R2668 and R2578, is switched to zero level.

The low-ohmic voltage divider, following the input impedance converter, attenuates 1, 2 or 5 times. Taking the overall combinations, together with the 1 or 10 times gain of the intermediate amplifier, twelve different deflection coefficients can be chosen.

To obtain the correct frequency characteristic, the attenuator sections are shunted by capacitors. Trimming capacitors provide for the adjustment of the capacitive divider sections for a.c. voltages to the same ratio of the resistive dividers for d.c. voltages. In this way, the divider sections are independent of frequency.
A diode clipper in the gate circuit of the field-effect transistor (FET V2451) protects it against excessive negative swings, the FET being inherently protected against excessive positive swings.

The high frequency path for the input signal consists of series capacitor C504 and the FET connected in a source-follower configuration. The low-frequency path comprises an operational amplifier and an error amplifier, which corrects the output signal related to the input signal of the impedance converter over a frequency range from d.c. to 1 kHz. The output of the error amplifier (D2416) is fed to the input of the operational amplifier to replace the missing low frequency portions of the signal. In this way, the drift is reduced to a minimum.

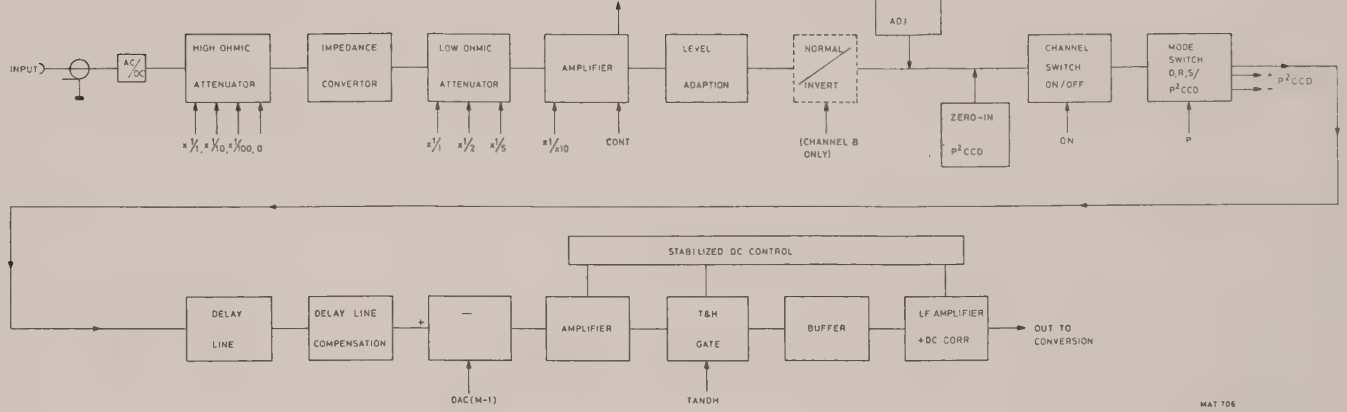


Fig. 6.2.72.

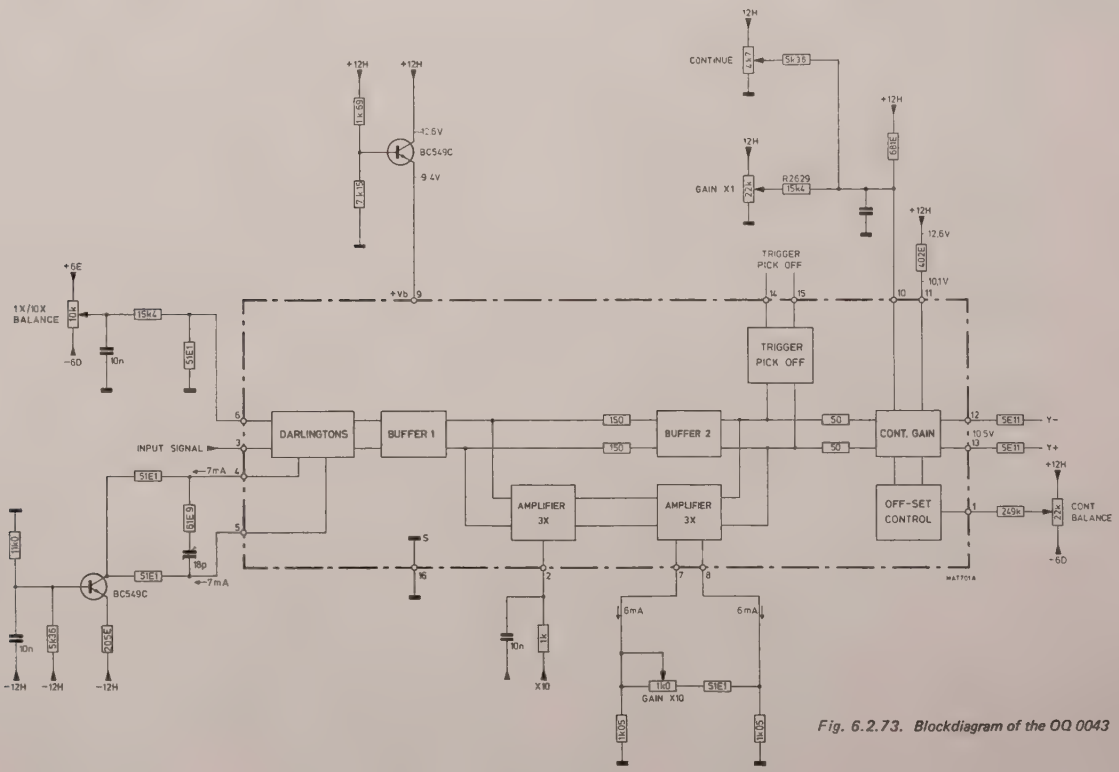


Fig. 6.2.73. Blockdiagram of the OQ 0043

The output of the impedance converter is applied to the 1, 2 or 5 times voltage divider. The dividing factors are controlled by FET switches (D2411), which in turn are controlled, via operational amplifiers (D2421), by the output ports of the microprocessor system.

6.2.21.3. Amplifier

a. Pre-amplifier

The output of the 1-2-5 divider stage is asymmetrically applied to pin 3 of pre-amplifier D2413 (OQ 0043) The block diagram of the OQ 0043 is given in the figure and is drawn with the relevant components as mounted in this oscilloscope.

The supply voltage is routed via a temperature-compensating circuit connected to pin 9. The OQ 0043 consists of input Darlington pairs to provide a symmetrical signal from the asymmetrical input; a buffer stage; two x3 amplifiers in series and switched in parallel to a buffer stage; trigger pick-off after amplification; a continuous gain adjustment facility and an offset adjustment for the continuous control.

b. Buffer stage

The output of the OQ 0043 is symmetrically applied to a buffer stage. In order to obtain the inverting mode for Channel B (PULL FOR –B), the buffer stage in this channel is provided with two extra transistors (V2419, V2424).
If the channel B invert switch is pulled, the microprocessor system decodes this setting and applies a high voltage to the base of V2408, which conducts.
Consequently, transistors V2418 and V2426 switch off and V2419 and V2424 now conduct so that the signal path is inverted.

After this stage, an offset stage, adjustable from the front panel, adapts the current so that an offset adjustment of four times the voltage range is possible (OFFSET A - V2456; OFFSET B - V2414).

To obtain the facility for switching both A and B channels to zero, necessary in the P^2CCD mode (see Section 6.2.8.3), both current flows are switched to the supply voltage via transistors V2469 and V2473. To control the zero switching, the Acquisition Control Logic and the time-base system generate the signals NUL IN and P respectively. These signals are applied to a NAND gate, the output of which is fed to operational amplifier D2422 (pins 8, 9 and 10). A zero on the negative input results in a high level on the output and the transistors conduct, thus interrupting the signal current flow.

6.2.21.4. Channel switch and mode switch

The principle of this oscilloscope is such that the channel A and channel B signal is always stored in the chopped mode. The CHOP signal, which is derived from the acquisition control logic (A9), is applied to the channel switch via NAND gates (D2428, D2429 on the logic circuit) to determine the positions of the ON/OFF switches. The signals derived from the control gates are called A ON and B ON, these signals being applied via V2468 (V2428) to pins 9 and 11 of D2412 (D2404). If the signal ON is high, the transistor blocks, and via V2474 (V2433), the outer transistors on the right-hand side of D2412 (D2404) become conductive. If the signal ON is low, V2468 (V2428) is conductive and the inner right transistors become conductive, the signal current flow of Y+ and Y– is shunted via pins 13 and 15 of D2412 (D2404), so the channel is switched off.

The following switching modes are indicated in the figures:

– Channel A ON: similar to channel A P^2CCD mode
– Channel B ON: similar to channel B P^2CCD mode } except for switching in D2409
– Channel A and B ON in ADD mode
– Dual channel P^2CCD mode (chopping is effected in P^2CCD)

In all modes except P^2CCD, chopping is effected by the channel switch.

To obtain a constant load for the supply voltages of the channel switch, it is necessary that the current remains the same, irrespective of the mode selected. Hence the reason for the alternative transistor loads. The relevant current paths are shown in the figures.

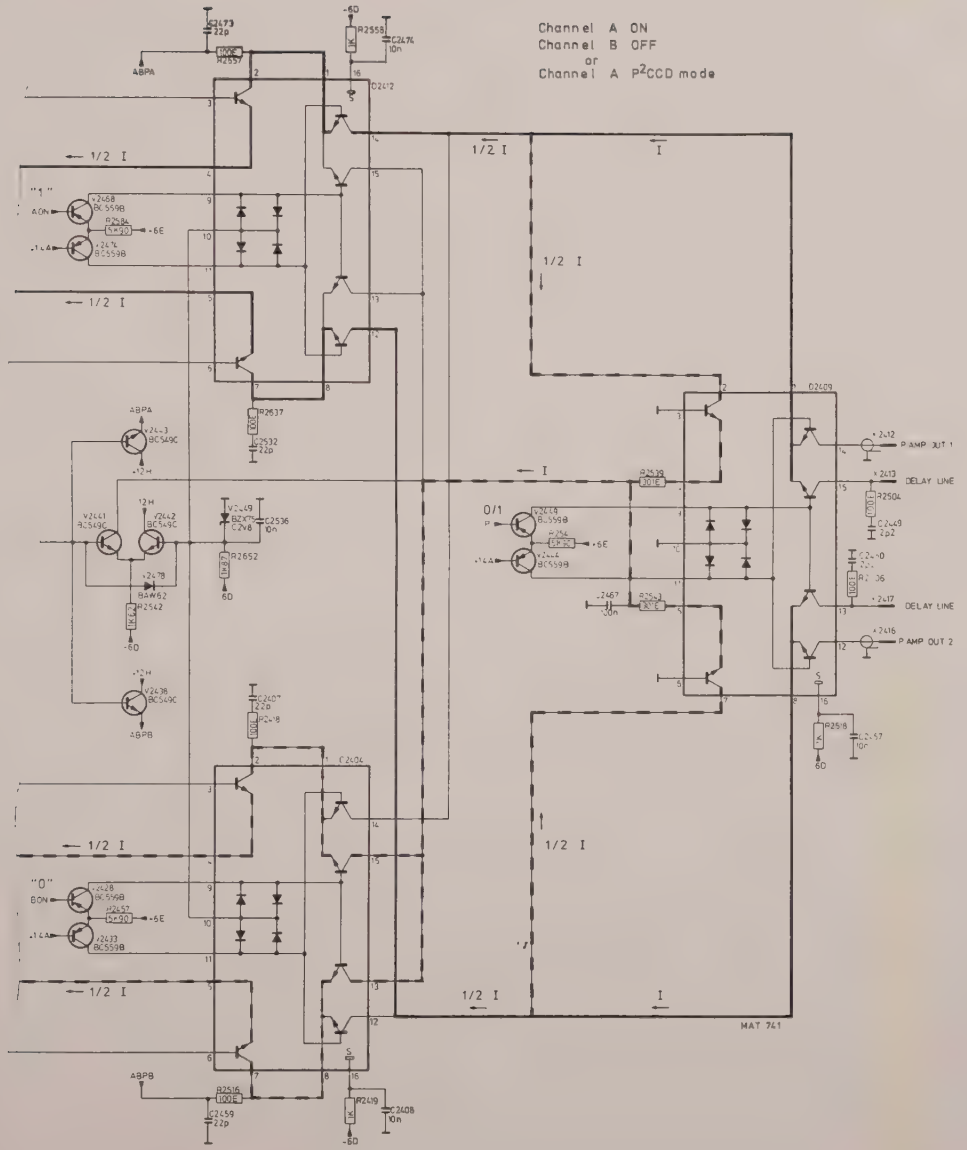


Fig. 6.2.75.

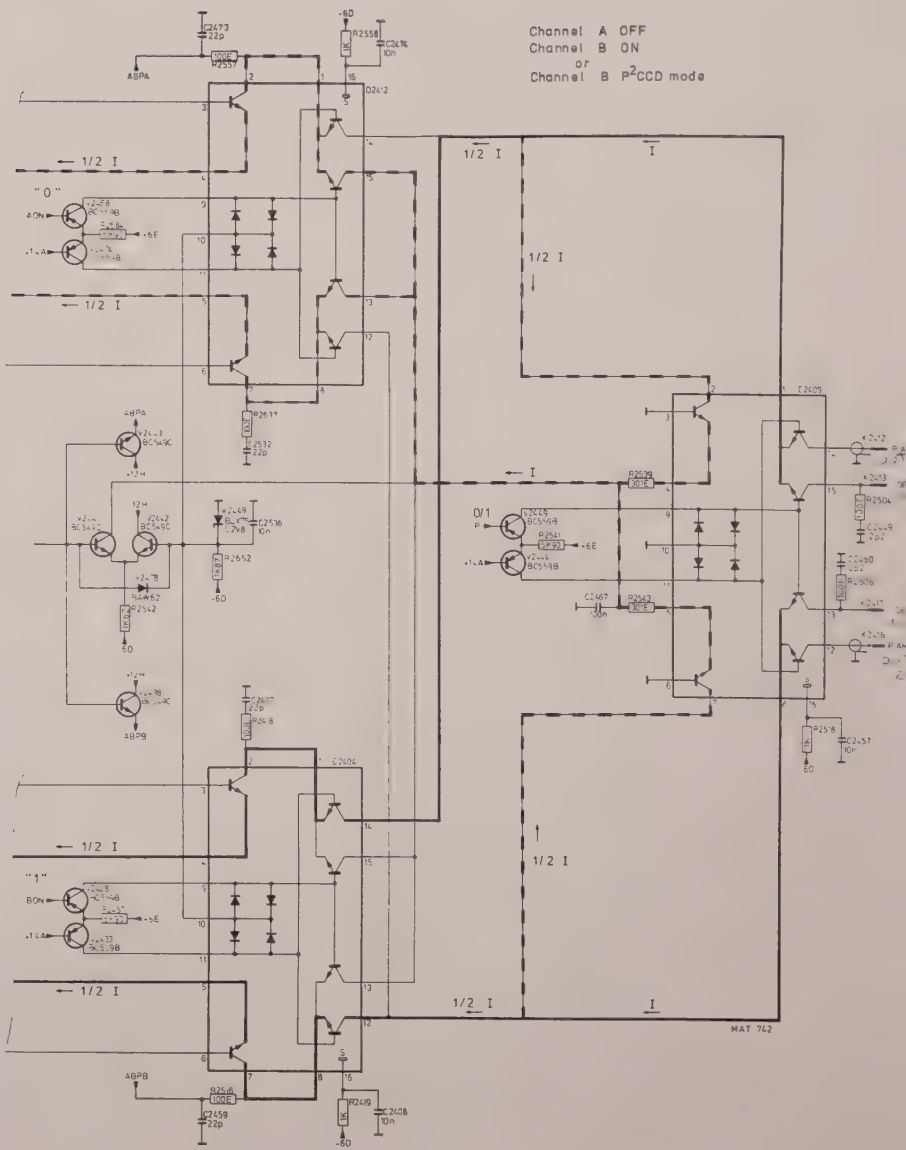


Fig. 6.2.76.

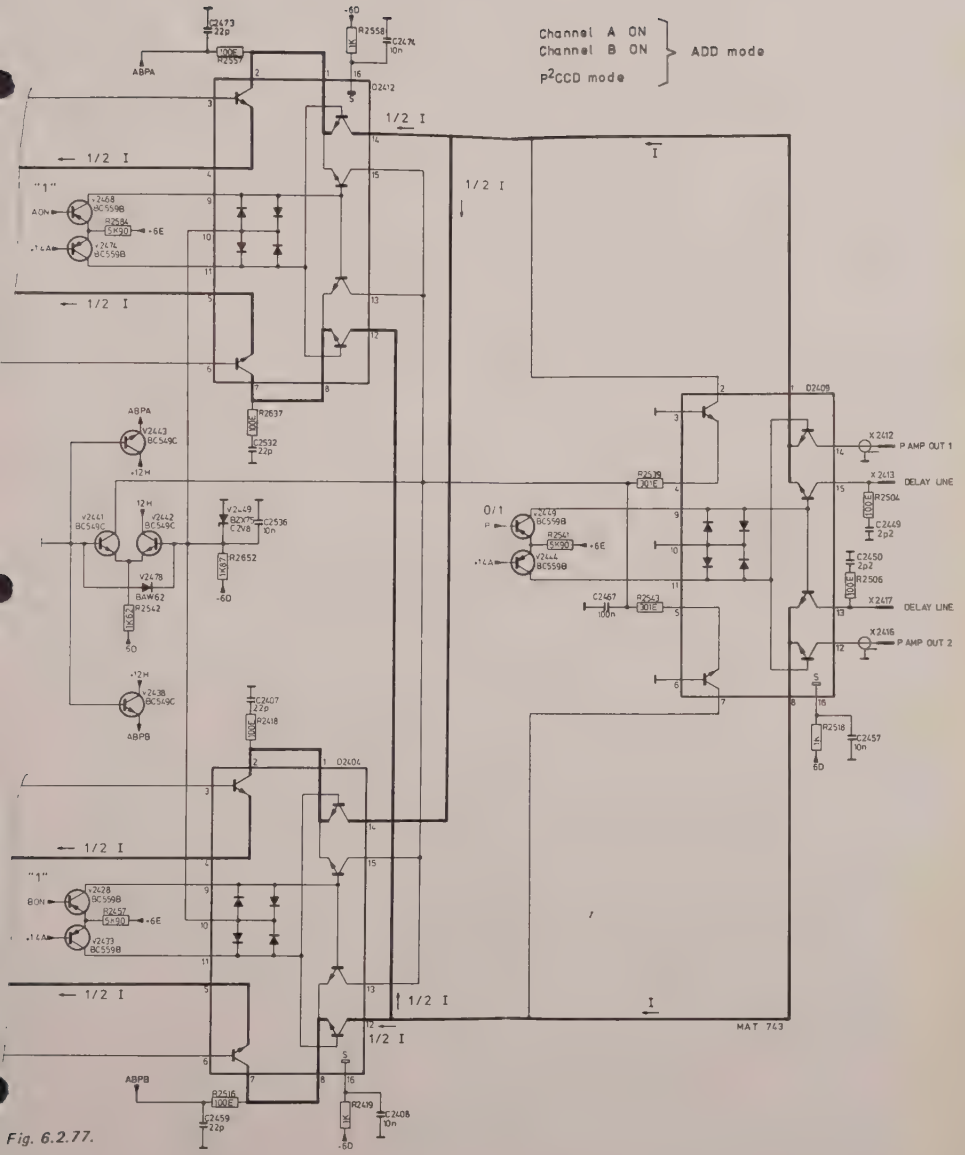


Fig. 6.2.77.

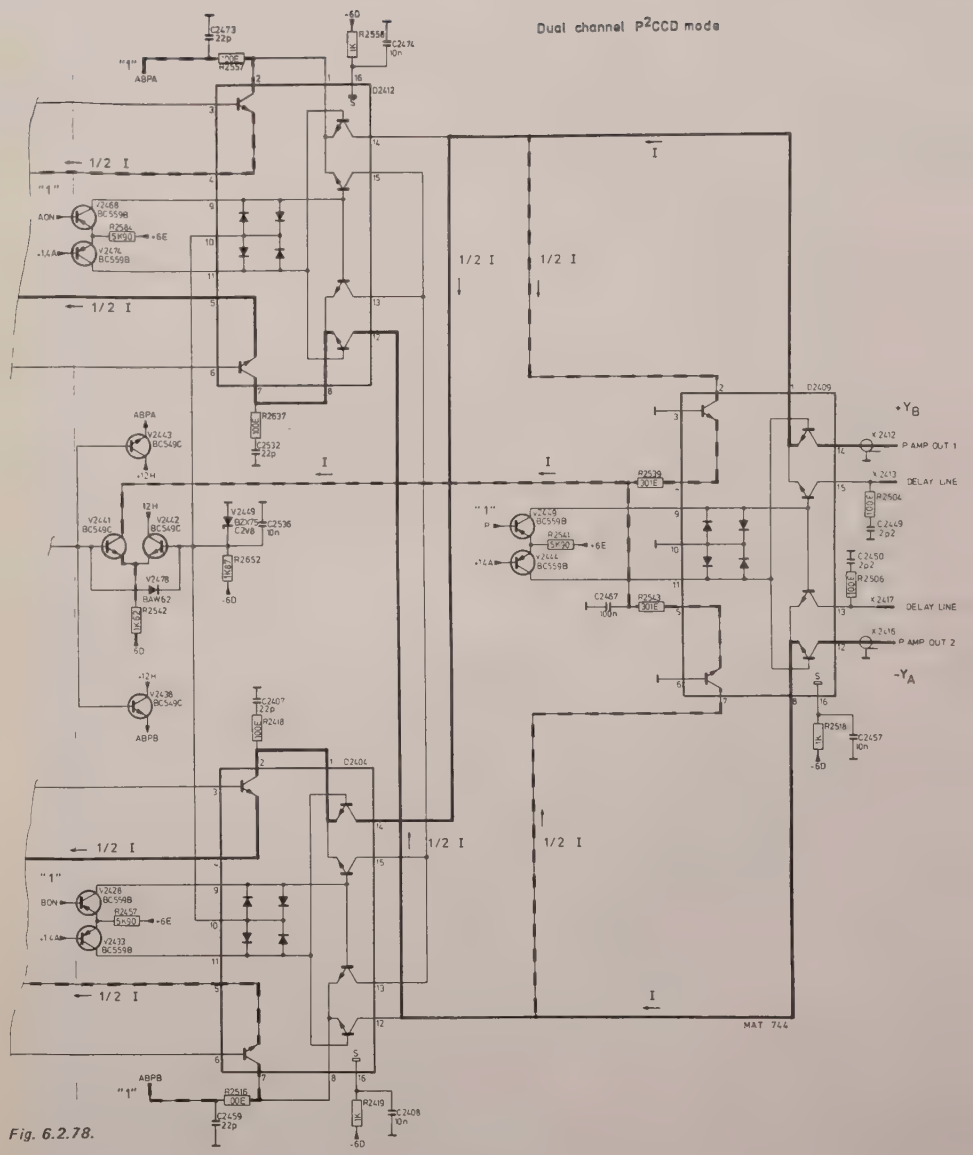


Fig. 6.2.78.

Integrated circuit D2409 serves to switch the signal either to the P2CCD amplifier or to the delay line.
If the signal P is high, the transistor V2449 blocks and V2444 becomes conductive. Consequently, the two outer right transistors of D2409 conduct and the signal is fed to the P AMP OUT 1 and P AMP OUT 2.
If the signal P is low, the two inner right transistors conduct and the signal is fed to the delay line. This occurs in the direct, roll and sampling mode.

6.2.21.5. Delay line compensation/Track and Hold Gate

A symmetrical delay line is mounted between the channel switch (via D2409) and a series feedback push-pull amplifier in combination with a shunt feedback push-pull amplifier.
The delay line is an symmetrically-mounted spiralled cable with characteristic impedance of 150 Ω and a delay of approximately 60 ns. The output is terminated by two series resistors, each of 75 Ω.

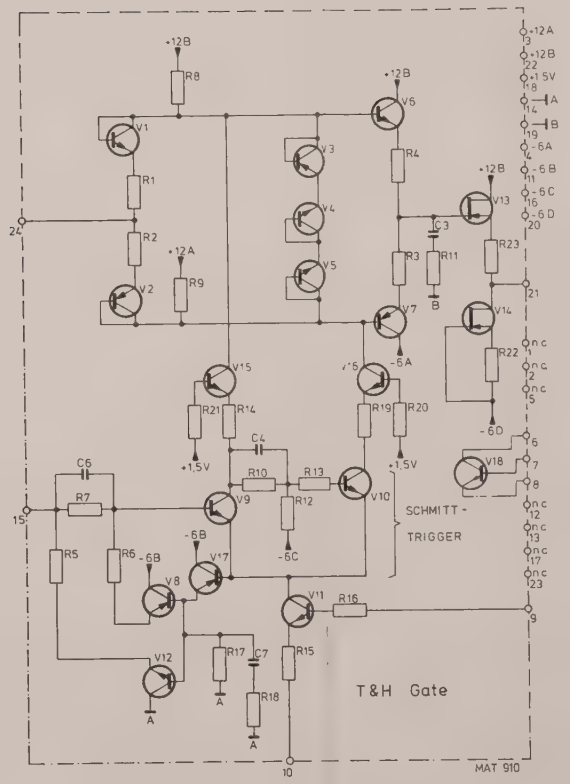
The emitter impedance of the series feedback stage (D3004) consists of RC frequency compensation networks.

For greater accuracy, it is preferable to measure the difference between an instantaneous analog signal sample and the previous signal sample rather than measuring each signal value separately.
This is done by recovering the previous sample that has been digitised, using a digital-to-analog converter and subtracting this value from the existing value to obtain the analog difference δV.

Transistors V3004 and V3003 are used to subtract the previous sample from the existing one. The sample to be subtracted, re-converted from the digital section, is called the DAC M-1. This voltage is converted into current and is applied to the emitter of the series feedback stage, D3004. As this signal is in antiphase it will be subtracted.

Because of the asymmetrical input to the Track and Hold (T & H) gate, the common-mode signal in addition to the supply voltage variation must be suppressed. For these reasons, the transistors V3001 and V3002 are introduced. The emitters are driven by a constant-current supply derived from the current source built up by an operational amplifier D3006 (pins 1, 2 and 3), which measures the voltage across resistor R3058 and drives V3008 to maintain constant current. The constant current drives transistors V3001, V3002 in such a way that the bias current is always constant.

The Track and Hold gate will now take a sample controlled by the signal TAND H. This signal is generated on the Trigger Unit A22. If the signal is low, the input signal is tracked. If the signal is high, the instantaneous value of the input signal is held momentarily. This gate is incapable of holding the sample long enough, without voltage droop, to convert it into a digital value. For this reason, a Sample and Hold gate is added on the Conversion Unit A8. The output signal of the Track and Hold gate is applied via a buffer amplifier to D3003, an operational amplifier (x5 gain approx.), which compensates the offset voltage. The output of the offset compensation circuit is applied via a multiplexer on the CCD logic unit A10 to the Sample and Hold gate on the Conversion Unit A8.



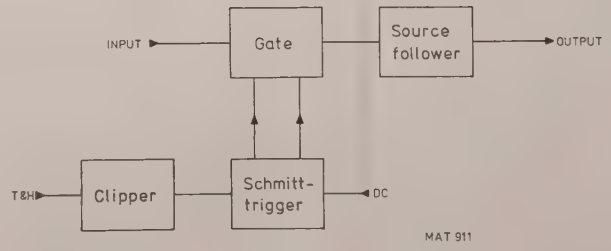
6.2.21.6. Logic circuits (control interfaces)

In order to activate the correct combination of reed relays, the microprocessor scans the following switches of both channel A and channel B:

AC/DC; 0 and AMPL/DIV switches.

To read the positions of the switches, an eight-input/four-output multiplexer (D2418) is addressed, each main loop by $\overline{IO0}$ together with read pulse $\overline{RD}$.
Address line A0 ensures that D2418 is addressed by address 801E for channel A switching and 801F for channel B switching.
The output of multiplexer D2418 and D2419 is connected to the data-bus lines D0 ... D7 and read by the microprocessor system.

The switch settings are converted by the microprocessor system and are applied, via the data-bus, to the latches D2424. These outputs ports are enabled by the combination of the write pulse $\overline{WR}$; the input/output pulse IO0, and for each port an address line (A1 and A2) Address D2424 is 8003. Address D2426 is 8005; address D2427 is 8006.
The outputs of these ports are fed to the reed relays; the following table indicates the reed relays that are active in relationship to the position of the switches:



RANGE (x10 probe)	RANGE (x1 probe)	K2412	K2413	K2414	K2416	K2418	K2409	K2411
.1 V	10 mV	I/O	1	1	0	0	0	0
.2 V	20 mV	I/O	1	1	0	0	0	0
.5 V	50 mV	I/O	1	1	0	0	0	0
1 V	.1 V	I/O	1	1	0	0	0	0
2 V	.2 V	I/O	1	1	0	0	0	0
5 V	.5 V	I/O	1	1	0	0	0	0
10 V	1 V	I/O	0	0	1	1	0	0
20 V	2 V	I/O	0	0	1	1	0	0
50 V	5 V	I/O	0	0	1	1	0	0
.1 kV	10 V	I/O	0	0	0	0	1	1
.2 kV	20 V	I/O	0	0	0	0	1	1
.5 kV	50 V	I/O	0	0	0	0	1	1
0	0	I/O	0	0	0	0	0	1

The complete output of D2424 (and D2426) with the corresponding attenuator, AC/DC and 0 switch positions is given in the table below (D2426 is for channel B and is analog):

RANGE (x10 probe)	RANGE (x1 probe)	x10A D6	$x^1/5A$	$x^1/2A$ D5	$x^1/1A$ D4	$x^1/100A$*	$x^1/100A$ D3	$x^1/10A$ D2	x1A D1	A-DC D0
.1 V	10 mV	1	1	0	1	1	1	1	0	–
.2 V	20 mV	1	1	1	0	1	1	1	0	–
.5 V	50 mV	1	0	0	0	1	1	1	0	–
1 V	.1 V	0	1	0	1	1	1	1	0	–
2 V	.2 V	0	1	1	0	1	1	1	0	–
5 V	.5 V	0	0	0	0	1	1	1	0	–
10 V	1 V	0	1	0	1	1	1	0	1	–
20 V	2 V	0	1	1	0	1	1	0	1	–
50 V	5 V	0	0	0	0	1	1	0	1	–
.1 kV	10 V	0	1	0	1	0	0	1	1	–
.2 kV	20 V	0	1	1	0	0	0	1	1	–
.5 kV	50 V	0	0	0	0	0	0	1	1	–
0	0	0/1	0/1	0/1	0/1	0	1	1	1	0
AC	AC	–	–	–	–	–	–	–	–	1
DC	DC	–	–	–	–	–	–	–	–	0

Range indication

When using a probe with range indication, the microprocessor system calculates the attenuation of the probe, which is then displayed on the scale rings of the AMPL/DIV switches and also in the alphanumeric display. The microprocessor system obtains the information of the probe, via D2417, by the signals $\overline{PA0}$, $\overline{PA1}$, $\overline{PB0}$, $\overline{PB1}$ for channels A and B respectively.
These signals are decoded in the microprocessor system and then applied to the displays.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
A∅-1-2		A4		Address bits from system address bus
ACON		A202		Slider of channel A continuous control
BCON		A202		Slider of channel B continuous control
CHOP		A9		Chopper signal
D∅ ... D7		A4		Data bits from system data bus
	D∅ ... D7	A21	A4	Data bits to system data bus
DAC M-1		A7		DAC M-1 output signal
	DRS	A21	A10	Signal information in D-R and S mode
$\overline{\text{ERUN}}$		A22		Enable run signal
$\overline{\text{IO∅}}$		A4		I/O address decoding signal
NULIN		A9		Signal to switch vert. ampl. input to zero
OFFA		A202		Slider of channel A OFFSET control
OFFB		A202		Slider of channel B OFFSET control
P		A12		P-mode signal
	PAMPOUT1	A21	A11	Output signal for P^{2}CCD
	PAMPOUT2	A21	A11	Output signal for P^{2}CCD
$\overline{\text{RD}}$		A4		Signal READ from microprocessor
$\overline{\text{RECURR}}$		A22		Signal from RECURR switch
$\overline{\text{ROLL}}$		A22		Signal from ROLL switch
$\overline{\text{RUN}}$		A22		Signal from R/S-RESET switch
$\overline{\text{SINGLE}}$		A22		Signal from SINGLE switch
$\overline{\text{TANDH}}$		A22		Track and hold signal
$\overline{\text{WR}}$		A4		Signal WRITE from microprocessor
+6 V		A15		
–6 V		A15		
+12 V		A15		
–12 V		A15		
⏚		A15		

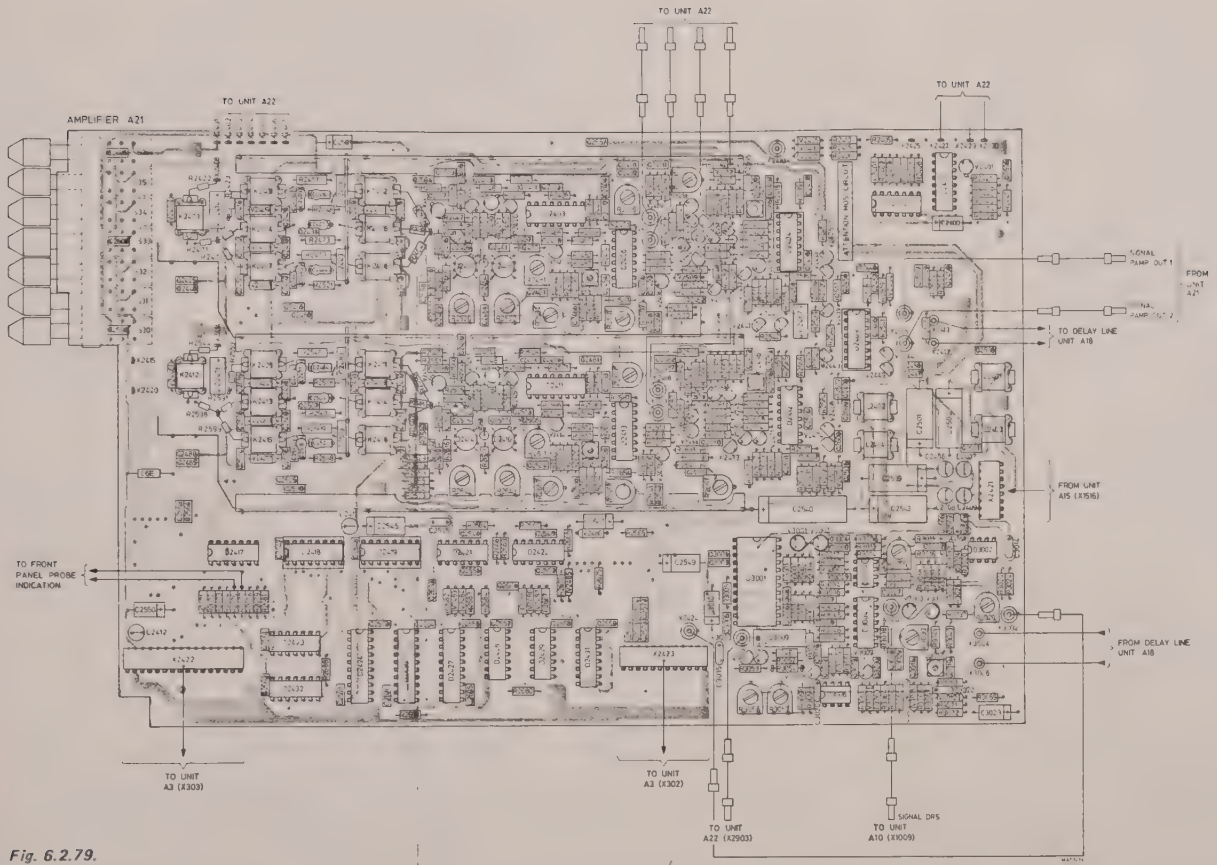
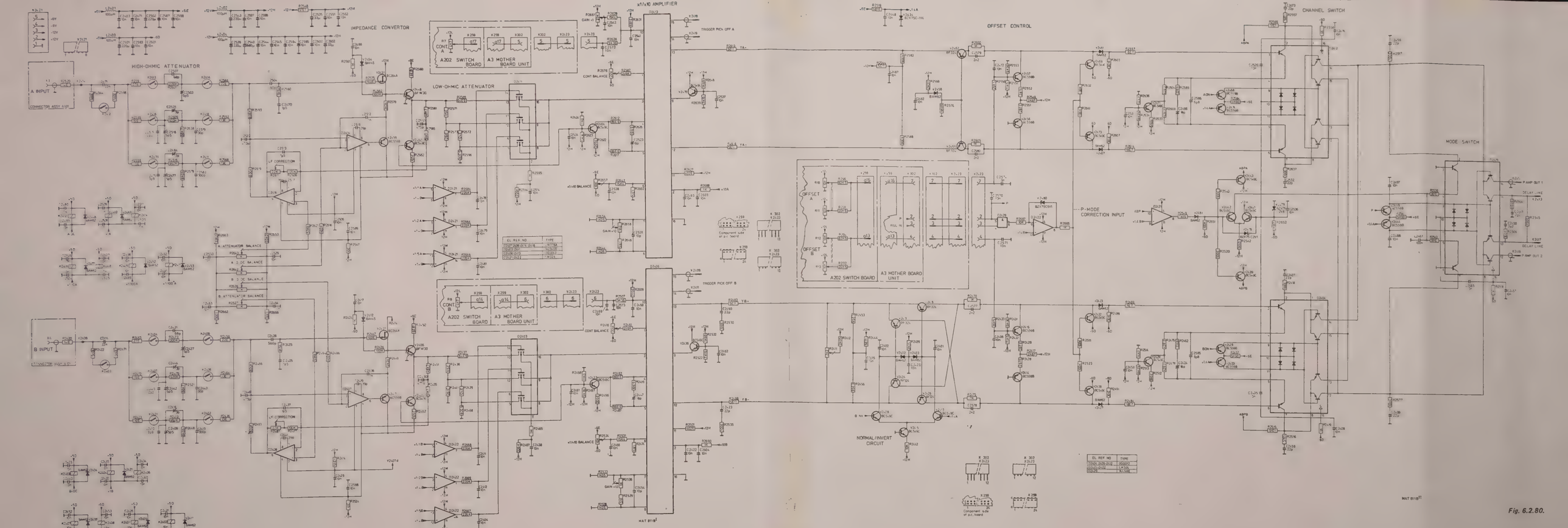

AMPLIFIER A21
TO UNIT A22
TO UNIT A22
TO UNIT A22
SIGNAL PAMP OUT 1
FROM UNIT A21
TO DELAY LINE UNIT A18
FROM UNIT A15 (X1516)
TO FRONT PANEL PROBE INDICATION
FROM DELAY LINE UNIT A18
TO UNIT A3 (X303)
TO UNIT A3 (X302)
TO UNIT A22 (X2903)
SIGNAL DRS
TO UNIT A10 (X1009)

Fig. 6.2.79.


IMPEDANCE CONVERTOR
HIGH-OHMIC ATTENUATOR
LOW-OHMIC ATTENUATOR
x1/x10 AMPLIFIER
A202 SWITCH BOARD
A3 MOTHER BOARD UNIT
A INPUT
B INPUT
OFFSET CONTROL
CHANNEL SWITCH
MODE SWITCH
P-MODE CORRECTION INPUT
NORMAL/INVERT CIRCUIT
TRIGGER PICK OFF A
TRIGGER PICK OFF B
MAT 8118
Fig. 6.2.80.

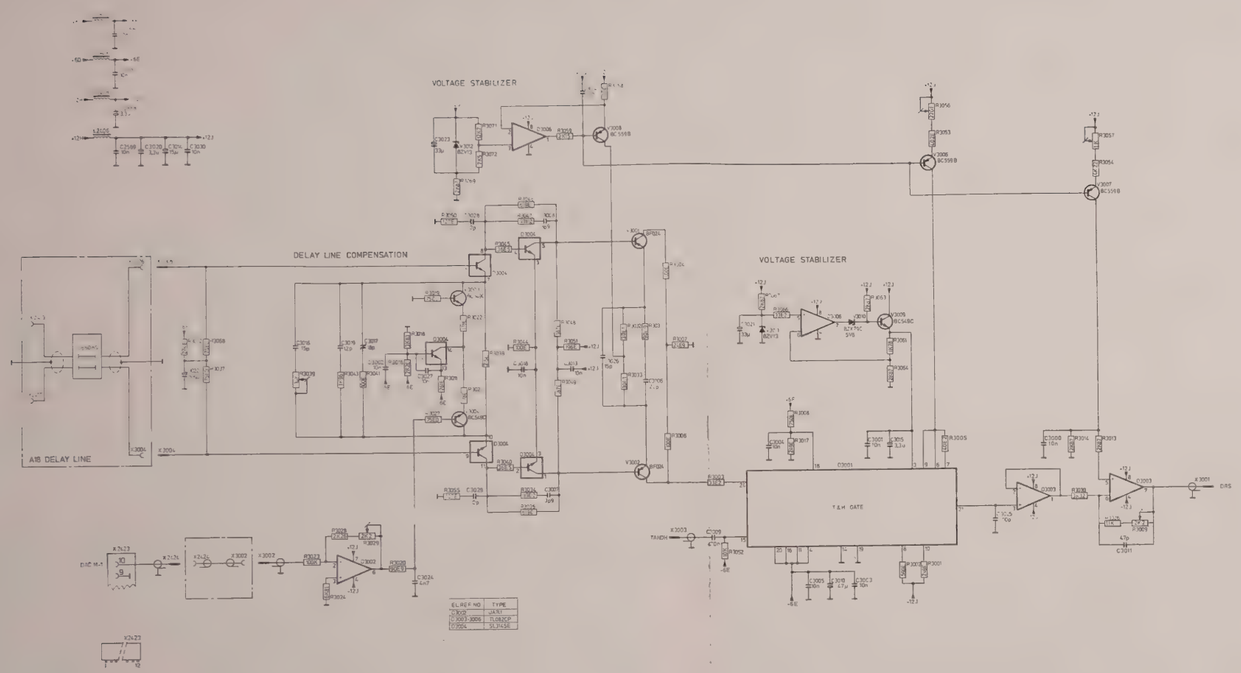


Fig. 6.2.81.

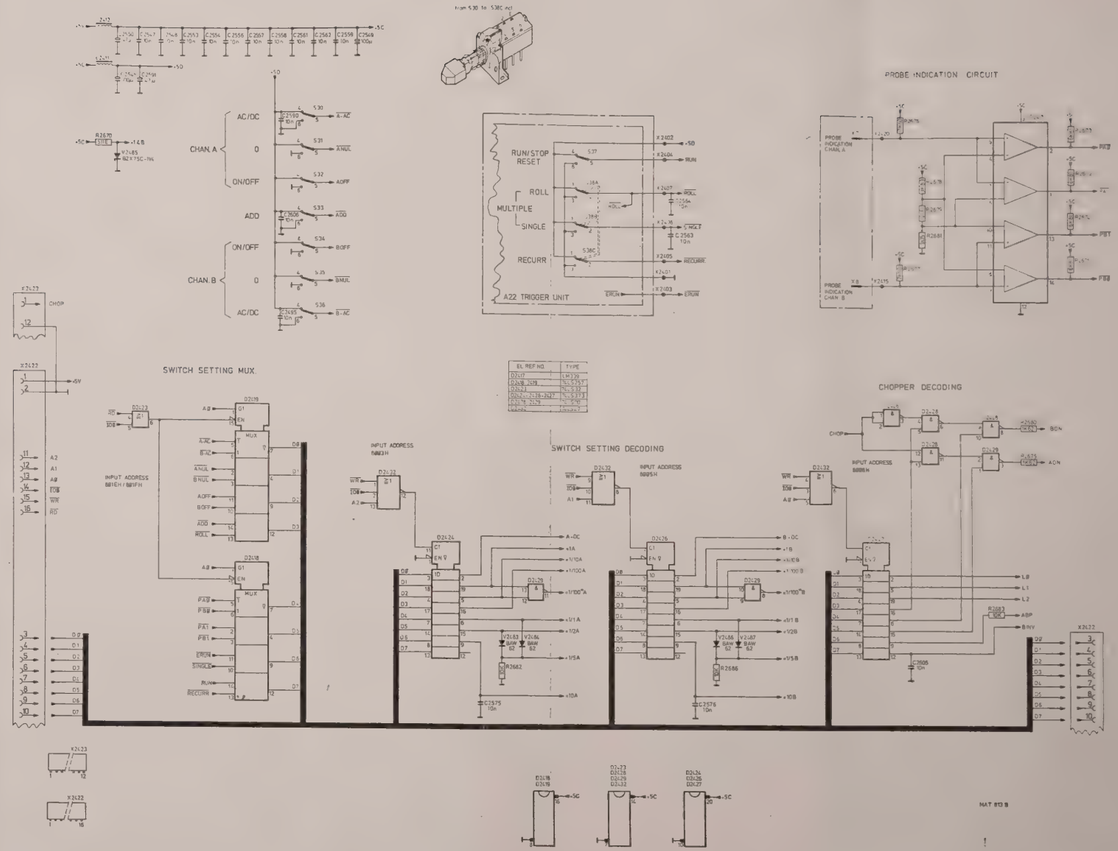


Fig. 6.2.82.

6.2.22. Trigger unit A22

The trigger unit comprises the following circuits:

- Trigger source switching circuit
- AC-DC coupling
- Peak-peak detector
- Level circuit
- Slope circuit
- TV circuit
- Pulse stretcher
- Time-base slow circuit
- Sampling circuit

6.2.22.1. Trigger source switching circuit

The trigger source switching circuit serves to detect the selected trigger source, the various possibilities being:

- channel A
- channel B
- LINE
- EXTERN
- EXTERN ÷ 10

With no pushbutton depressed, channel A is automatically chosen. Transistor V2723 provides this facility.
If all pushbuttons are released, the base of V2723 is connected to zero, which causes the transistor to block.
In turn, transistors V2746 and V2747 are blocked and therefore the signal of channel A is enabled.
In all other positions of the switches, except for CHAN A switch, V2723 is conductive and the channel A signal flows via V2746 and V2747 to the –6 V supply line, i.e. it is blocked.

In single or recurrent operation, two modes of external triggering are possible: EXT and EXT ÷ 10.
In the EXT ÷ 10 mode, the input signal is attenuated by a factor of 10 and applied to the amplifier. The h.f. path of the amplifier is via C2708 and V2701 to V2702; the l.f. path is a.c.-coupled via C2719 and D2708 to V2702, and d.c.-coupled via D2709 (13, 14) and D2708 to V2702.

In the roll-mode the function of the external input is a RUN/STOP action at TTL-level. This is a software OR-function together with the position of the R/S switch. A high level at the input is applied to V2727 via D2709 and D2708, V2702, V2707. This causes the ERUN signal to go high, which then starts the ROLL-mode via the software program if the R/S switch is at STOP.

6.2.22.2. AC-DC coupling

The trigger signal is routed to V2724 and V2729 via the AC-DC coupling circuit.
If the d.c. signal is high, the reed relay K2701 switches off and the signal is applied to the bases of V2724 and V2729 via R2789, R2788 and R2792, R2791 respectively. If the d.c. signal is low, the reed relay is energised and the d.c. component in the trigger signal is filtered out, the a.c. component flowing through C2737 and C2743. The signal is applied via an amplifier stage to the input of the slope circuit and the input of the peak-peak detector.

6.2.22.3. Peak-peak detector

A peak-to-peak detector is introduced to enable the possibility of levelling between the positive and negative peaks of the signal in the AUTO mode.
The positive peak flows via the base-emitter diode of D2703 (6, 7, 8), to charge electrolytic capacitor C2709. The current required to drive D2703 (9, 10, 11) is obtained from D2704 (5, 6, 7). The output of this amplifier is the d.c. level proportional to the positive peak.
The negative peak flows via the emitter-collector diode of D2703 (1, 2, 3) to charge C2711. This peak voltage is amplified by D2704 (1, 2, 3) to give an output d.c. level proportional to the negative peak.

6.2.22.4. Level circuit

The level potentiometer is connected to the outputs of a multiplexer D2701.
Depending on the signals TV and OH, the level potentiometer is connected to:

MODE	D2701 OUTPUTS 13	3	TV	OH
AUTO	postop	negtop	0	0
DCor AC	d.c.	d.c.	0	1
TV +	postop	postop	1	0
TV −	negtop	negtop	1	1

6.2.22.5. Slope circuit

The trigger signal is applied to the differential amplifier in D2711.
The output of the level circuit is applied to the other input.
Depending on the position of the slope switch, either V2732 or V2751 conducts, which causes the positive or negative signal to be connected to the outputs of D2711. The trigger signal is applied via an electronic switch V2761 and its associated components to ECL-Schmitt trigger D2907 (2, 3, 4, 5).

6.2.22.6. TV circuit

The outputs 12 and 13 of D2711 are applied to the video clipper consisting of V2717 and its components.
The TV trigger signal is now applied to two re-triggerable monostable one-shots (D2702) in series, with different pulse times. The output of the first one-shot is applied to the clock input of D-flip-flop D2707. This flip-flop is enabled by the TV signal. At output 9 of D2707 a 50 Hz field pulse is available. To obtain frame pulses, the inverting output 8 of D2707 is applied to clock input 3. At the D input 2, the output of the second one-shot is applied. The frame pulse now appears at the inverting output 5 of D2707.
Normal triggering is now inhibited because of the TV signal applied to the electronic switch V2761, which causes the voltage at X2708 to go low.

6.2.22.7. Pulse stretcher

The trigger pulse is applied via the ECL-Schmitt trigger to the clock input of the dual ECL D-flip-flop D2904.

This flip-flop in combination with two Schmitt trigger circuits D2907 (9, 10, 6, 7), D2907 (12, 13, 14, 15) form the pulse stretcher.
The principle is shown in the following diagram.

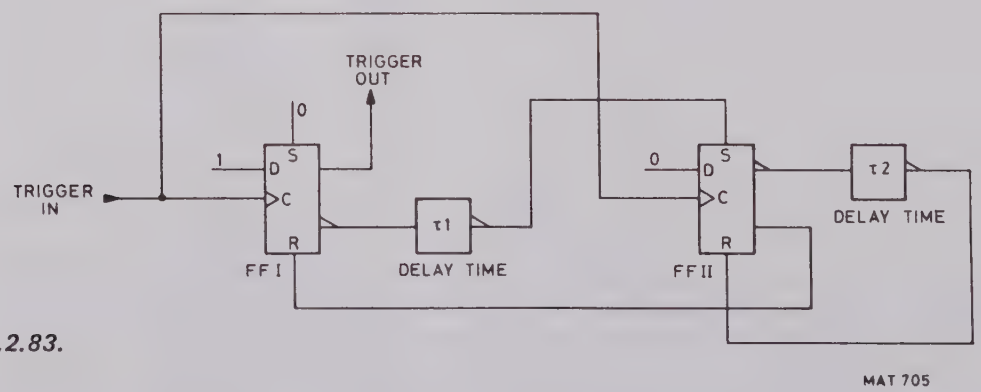


Fig. 6.2.83.

On receipt of a trigger pulse at the clock input of FFI, its inverted output goes low. After time t_1, this output is applied as a logic high signal, which sets FFII. Consequently, its inverted output goes low and the non-inverting output goes high. This results in a reset of FFI. After t_2, FFII is reset and, as a result, FFI is enabled.

Times t_1 and t_2 are chosen so that the pulse stretcher acts as a pulse-shaper at frequencies up to 2 kHz, as a divide-by-two circuit from 2 kHz to 10 kHz, and as a divider by n for frequencies above 10 kHz.

6.2.22.8. Time-base slow circuit

The output of the pulse stretcher is converted to TTL-level by the two converters D2906. The upper converter produces the TRIST signal which is applied to the delayed trigger unit A13. In the sampling mode, the lower converter can feed the trigger signal to the sampling system.

In the Direct and Roll-modes, the system is operated by the TBS signal. This signal is fed via inverter D2911 (5, 6) and NAND-gate D2912 (11, 12, 13) to the clock input 11 of D-flip-flop D2909. At the inverted output 8, a low level is clocked, which is the STOP signal. This STOP signal is applied to multiplexer D2908 and via the inverted output and diode V2919 to the wired-OR gate (D2911-13). Pin 12 of D2911 goes low and via the upper NAND-gate of D2902 a Track and Hold (TANDH) pulse is generated.

The lower NAND-gate of D2902 is controlled by the TANDH pulse via D2903 (13, 11) and inverter D2911 (1, 2) and generates a HONCONDRS pulse. At the same moment, a TANDH pulse is taken over by a high level at output 8 of D2903.

The HOCONDRS pulse goes high after 3.6 μs caused by the RC combination R2928 and C2918, C2919. After approximately 0.4 μs, output 8 of D2903 goes low and therefore the HOCONDRS pulse again becomes low.

6.2.22.9. The sampling circuit

If the oscilloscope is in the sampling mode, the output of the pulse stretcher is applied to the clock input 11 of D2909. This flip-flop is enabled by a high level on reset input 13, and its inverted output blocks transistors V2916 and V2913.
Sawtooth capacitor C2923 starts charging with a current derived from the current source V2922. The current that feeds the fast ramp sawtooth generator is determined by the settings of the time-base switch. These settings are decoded by the microprocessor system and applied to a FET-switch array D2401 and FET V2401, via D2402. The following table shows the relationship between the time-base settings and the current-source control FETs.

	D2431					D2431		
	4	5	11	6	7	L2	L1	LØ
5 ns/cm	1	1	0	1	1	1	1	0
10 ns/cm	1	0	1	1	1	0	0	1
20 ns/cm	1	1	1	0	1	1	0	0
50 ns/cm	1	1	1	1	0	1	0	1
.1 μs/cm	0	1	1	1	1	0	0	0
.2 μs/cm	1	1	1	1	1	1	1	1

Except for the .2μ/div, one control line is always low. This means that one of the resistors R2421, R2443, R2446, R2454 and R2458 is switched in parallel with the current-determining resistor R2434. The value of the resistors is determined so that in the 5 ns/cm position the highest current is obtained.
The fast ramp sawtooth voltage is applied to the positive input of comparator D2902 (11, 12). To the negative input, a preset voltage built-up from DACSTAIR and DACDEL is applied. If the last ramp reaches the potential of the preset voltage, the comparator output goes low and the triple-NAND gate goes high for 4 μs (described under time-base slow).
The sawtooth voltage is blocked and the capacitor is discharged by a reset pulse derived from the TANDH pulse at D2909-13, so output 8 goes high.
The flip-flop is enabled to start a new sawtooth ramp if the TANDH signal is low and TRACK is high.
The DACSTAIR signal is generated at the ACL unit and is divided into 256 steps, each of 40 mV. The DACDEL signal is generated on the delayed time-base unit and is divided into 200 steps, each of 40 mV. This means that each division delay corresponds to two steps (i.e. 80 mV). The resistor network R2910, R2913, R2914 is chosen so that 256 steps of DACSTAIR generate the same potential as 20 steps of DACDEL at input 6 of D2901.
If no sampling mode is chosen, the TANDH signal is not generated by means of the sawtooth generator and the comparator, but via the system described under time-base slow. This is effected by presetting the negative input 11 of the comparator to a high voltage via D2901.

INCOMING SIGNAL	OUTGOING SIGNAL	GENERATED ON UNIT	USED ON UNIT	DESCRIPTION
	AUTO TB	A22	A13	Auto signal from AUTO switch
DAC DEL		A13		Output signal of DAC delay
DAC STAIR		A9		Output signal of DAC STAIR
	ERUN	A22	A21	Enable run signal
FRUN		A13		Freerun signal
	HOCONDRS	A22	A9	Hold and convert signal in D-R and S-mode
LINE		A15		Signal for mains triggering
S		A12		S-mode signal
	TANDH	A22	A21	Track and hold signal
TBS		A12		Time-base slow
TRACK		A9		Track command for S/H circuit
	TRIST	A22	A13	Trigger signal for strecher
+5V		A15		
–5.2V		A15		
+6V		A15		
–6V		A15		
+12V		A15		
–12V		A15		
+40V		A15		
▬		A15		

TEST POINTS	
X2700	External trigger
X2707	TRIGGER SIGNAL
X2708	TRIG.
X2905	HOCONDRS

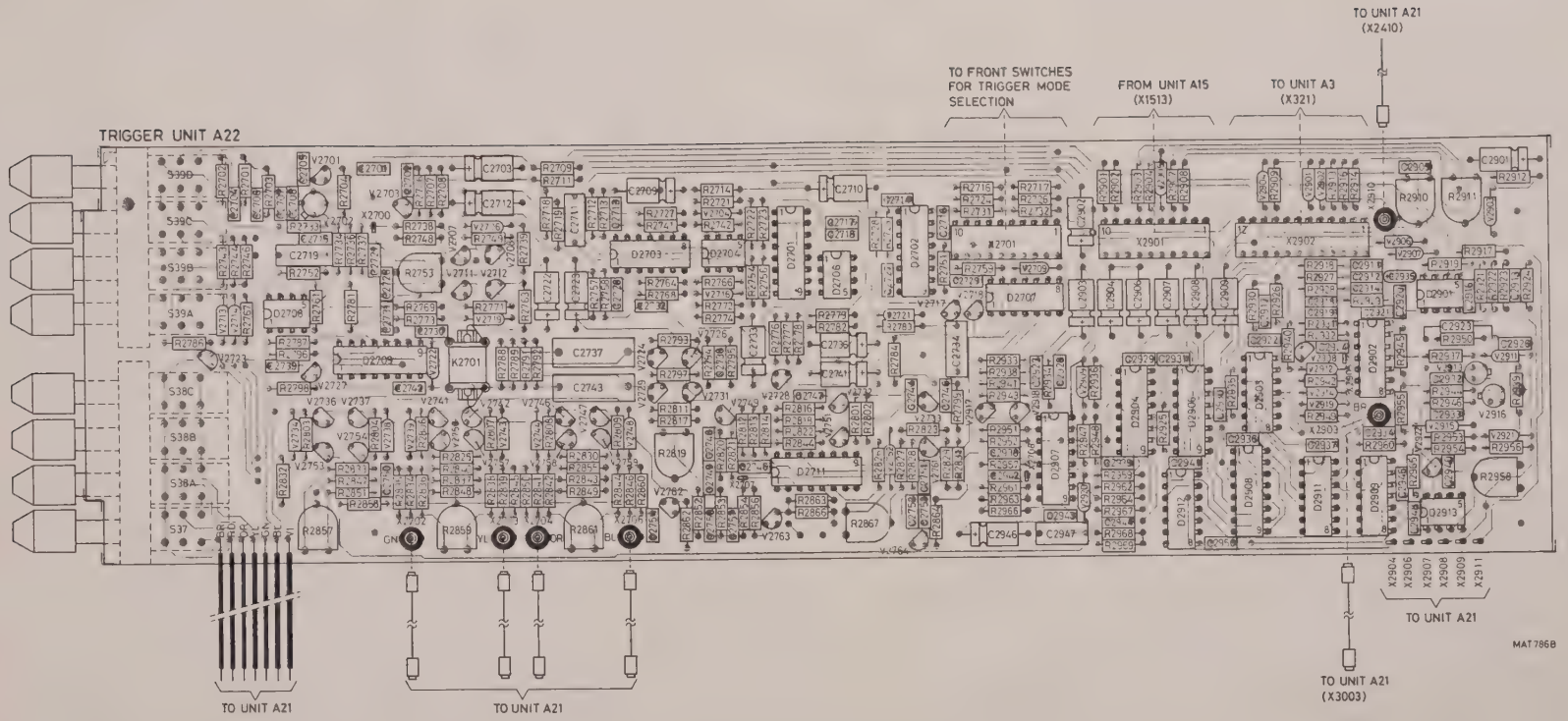
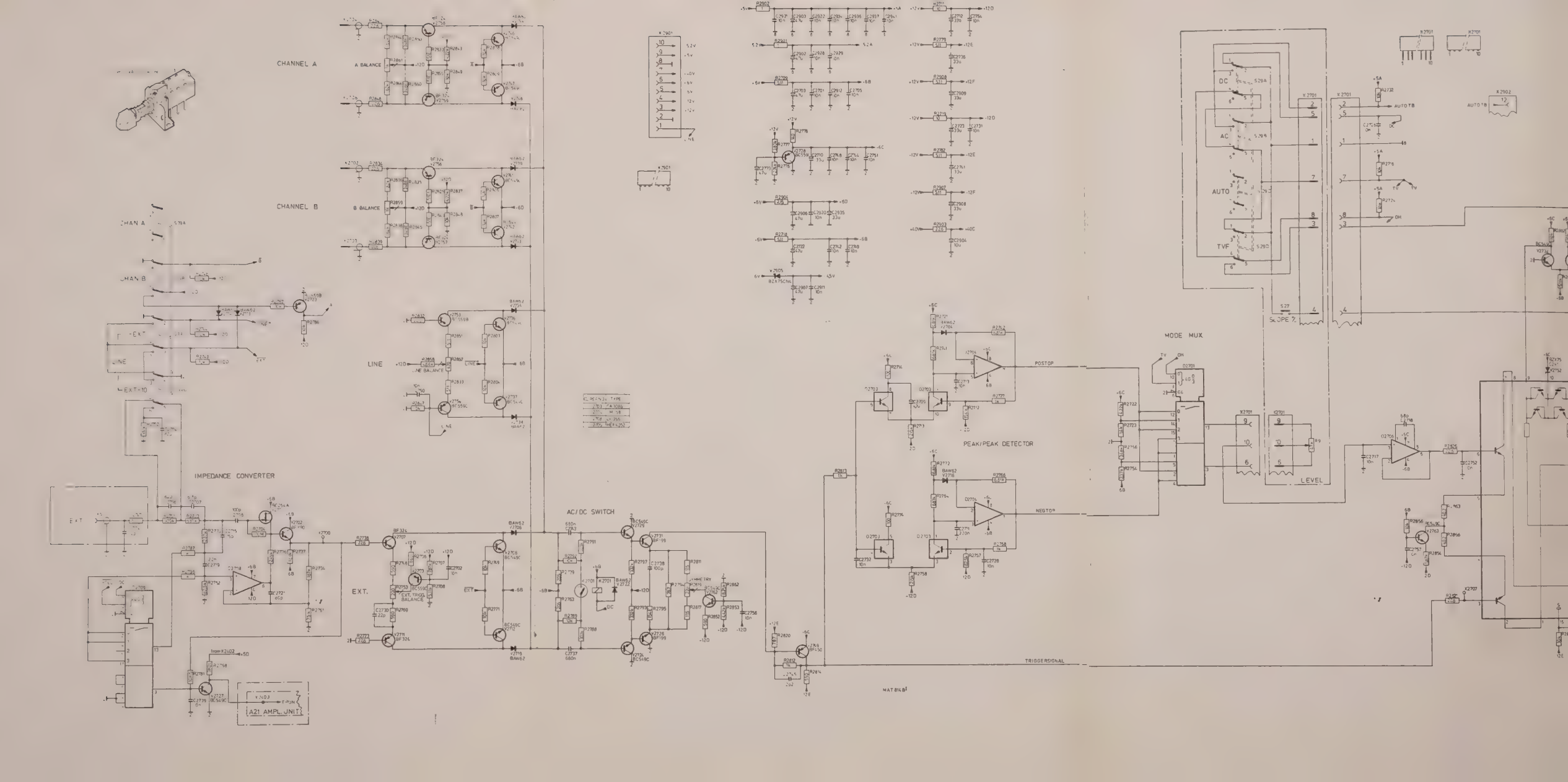

TRIGGER UNIT A22
TO FRONT SWITCHES FOR TRIGGER MODE SELECTION
FROM UNIT A15 (X1513)
TO UNIT A3 (X321)
TO UNIT A21 (X2410)
TO UNIT A21
TO UNIT A21
TO UNIT A21 (X3003)
MAT 786B

Fig. 6.2.84.


CHANNEL A
A BALANCE
CHANNEL B
B BALANCE
CHAN A
CHAN B
LINE
LINE BALANCE
IMPEDANCE CONVERTER
EXT.
EXT. TRIGG. BALANCE
AC/DC SWITCH
PEAK/PEAK DETECTOR
POSTOP
NEGTOP
MODE MUX
LEVEL
DC
AC
AUTO
TVF
SLOPE
TRIGGERSIGNAL
A21 AMPL. UNIT

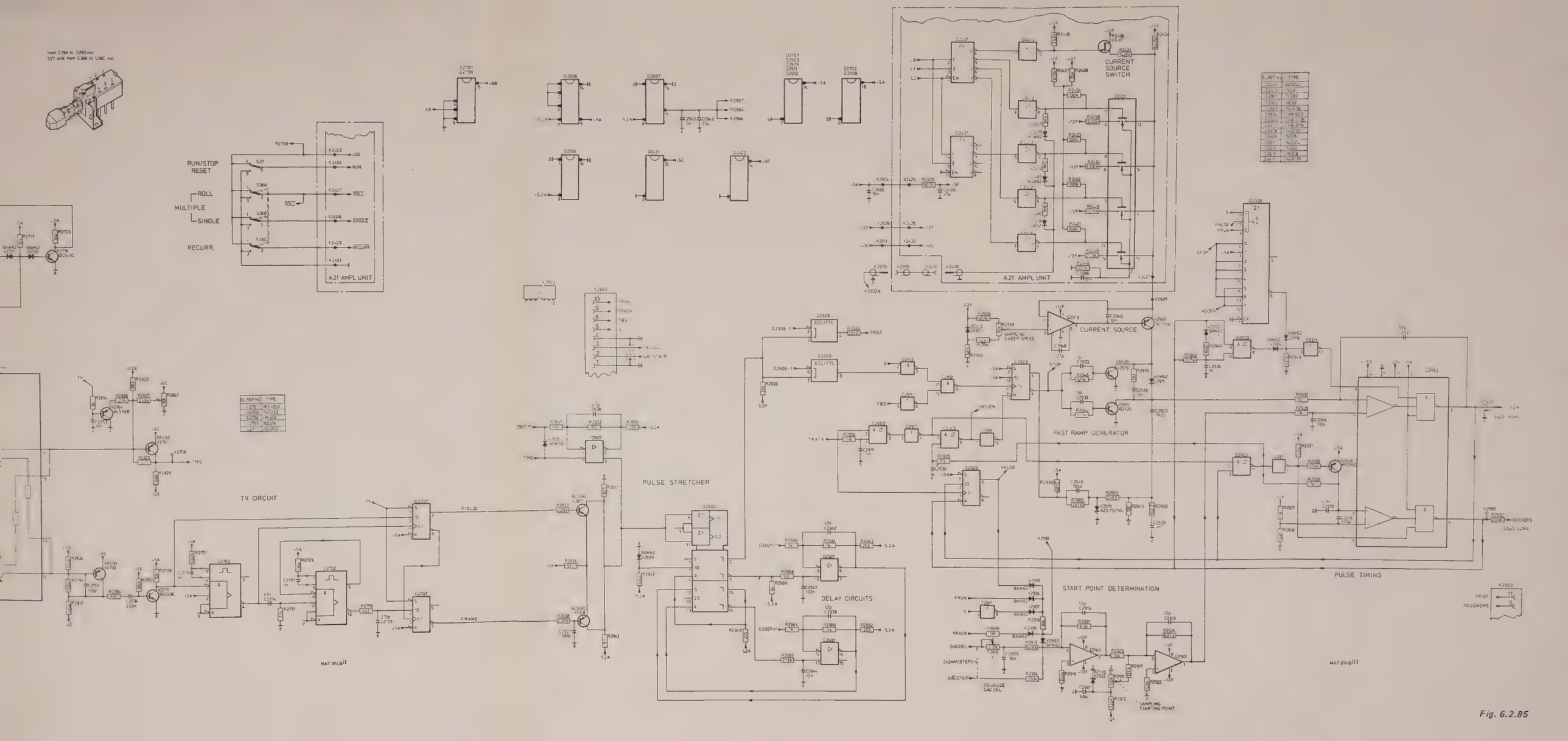

RUN/STOP
RESET
ROLL
MULTIPLE
SINGLE
RECURR.
A21 AMPL UNIT
CURRENT SOURCE SWITCH
A21 AMPL UNIT
CURRENT SOURCE
FAST RAMP GENERATOR
PULSE STRETCHER
TV CIRCUIT
FIELD
FRAME
DELAY CIRCUITS
START POINT DETERMINATION
PULSE TIMING
TRIST
HOCONDRS
MAT 814B II
MAT 814B III

Fig. 6.2.85

6.2.23. EHT unit A23

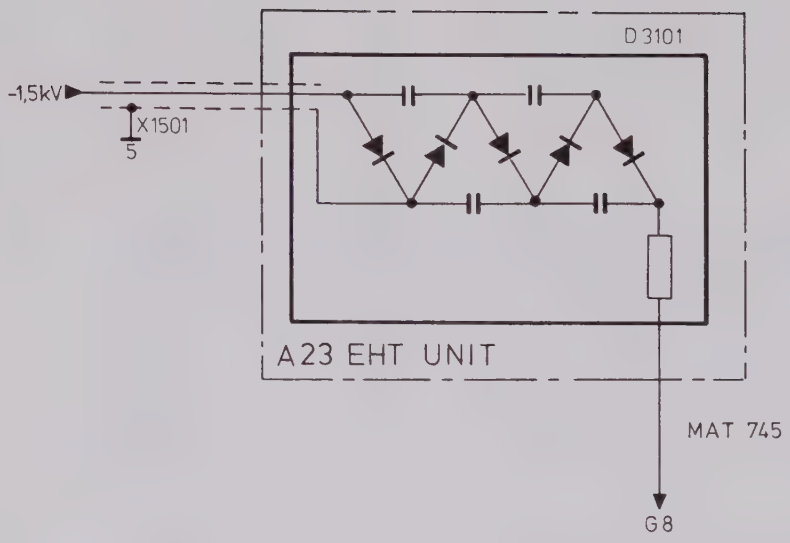


Fig. 6.2.86

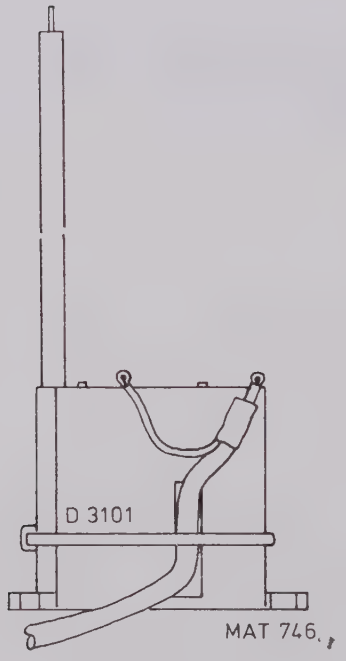


Fig. 6.2.87

7. DISMANTLING THE INSTRUMENT

7.1. WARNINGS

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

ATTENTION: This section provides the dismantling procedures required for the removal of components during repair operations. All circuit boards removed from the oscilloscope should be adequately protected against damage, and all normal precautions regarding the use of tools must be observed. During dismantling procedures, a careful note must be made of all disconnected leads that they may be reconnected to their correct terminals during assembly. Damage may result if the instrument is switched on when a circuit board has been removed, or if a circuit board is removed within one minute after switching off the instrument.

WARNING: The E.H.T. cable is unbreakably connected to the E.H.T. unit (disconnection at C.R.T.). When the E.H.T. cable to the post-acceleration anode of the C.R.T. is disconnected at the C.R.T. unit end, the E.H.T. cable must be discharged immediately by shortening them to earth.

7.2. REMOVING THE COVERS

To remove the instrument covers, proceed as follows:

– Both upper and lower cabinet plates can be removed after slackening the four quick-release fasteners at the corners of each plate. To prevent the fasteners coming apart, do not slacken more than two turns.

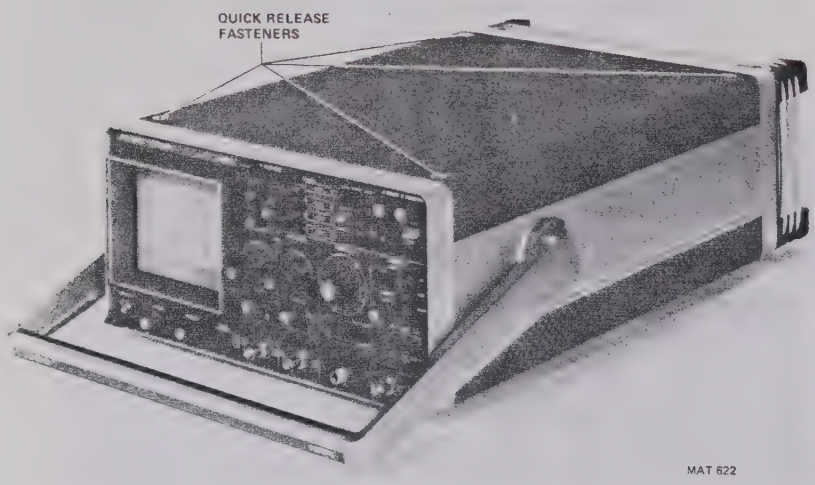


Fig. 7.2.1. Removing the instrument covers.

7.3. ACCESS TO PARTS FOR CHECKING AND ADJUSTING PROCEDURE

Adjusting elements are accessible after removing the instrument covers.
Only for measurements and adjustments on the AC POWER unit A16 and DC POWER unit A15 the rear panel has to be removed.

Remove the six screws that secure the rear panel to the instrument

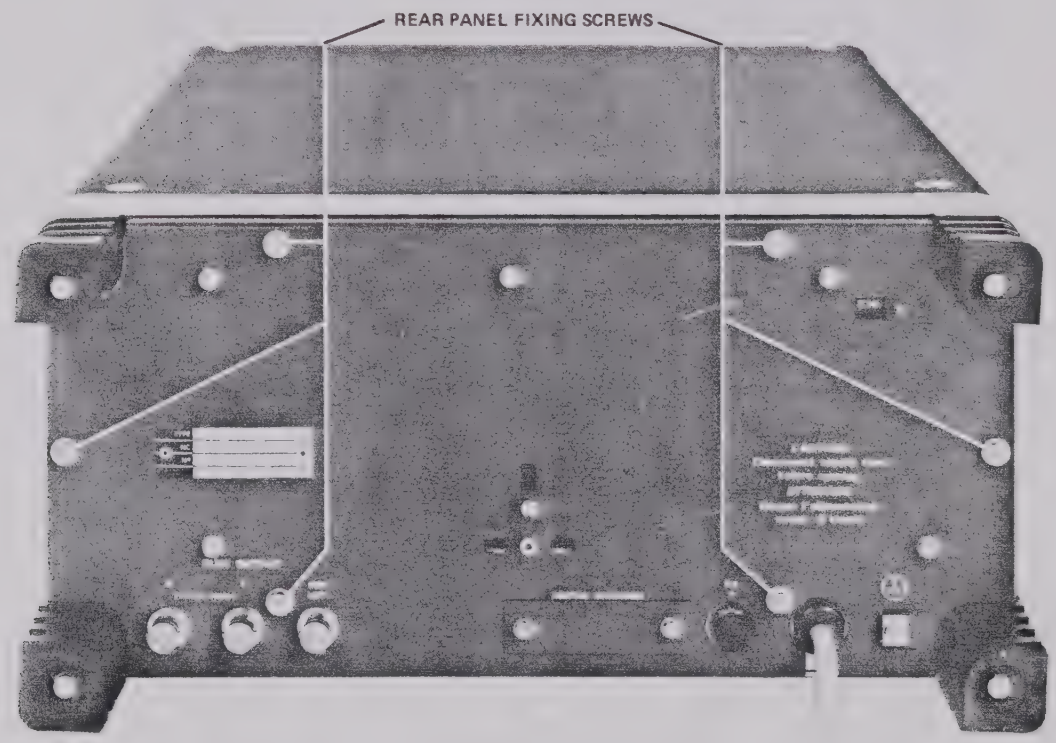


Fig. 7.2.2.

Unit A16 which is mounted on the rear panel can be placed outside the instrument by pulling the rear panel.

For better access to unit A15 both the upper and lower screening plates can be removed.

8. CHECKING AND ADJUSTING

Before starting with the CHECKING and ADJUSTING procedure check the instruments specification by means of the PERFORMANCE CHECK procedure on page 8-29.

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

8.1. GENERAL INFORMATION

The following information provides the complete checking and adjusting procedure for the oscilloscope. As various control functions are interdependent, a certain order of adjustment is often necessary.
The procedure is, therefore, presented in a sequence which is best suited to this order, cross-reference being made to any circuit which may affect a particular adjustment.
Before any check or adjustment, the instrument must attain its normal operating temperature.

- Where possible, instrument performance is checked before an adjustment is made.
- Warming-up time under average conditions is 30 minutes.
- All limits and tolerances given in this section are calibration guides and should not be interpreted as instrument specifications unless they are also published in chapter 1.2. characteristics.
- Tolerances given are for the instrument under test and do not include test equipment error.
- The most accurate display adjustments are made with a stable, well-focused, low-intensity display. Unless otherwise noted, adjust the Intensity, Astigmatism, Focus and Trigger Level controls as needed.

8.1.1. Recommended test equipment

Type of instrument	*Specifications*	*Used for*	*Example of recommended instrument*
1. Constant amplitude sine-wave generator	Freq. 200 kHz ... 60 MHz Constant amplitude of 12 mVp-p ... 1.2 Vp-p	Bandwidth check of vertical channels and triggering	Tektronix SG 503 + SG 504
2. Time marker generator	Repetition rate 0.5 s ... 20 ns	Checking and adjusting of sweep rates	Tektronix TG 501
3. Square-wave calibration generator	Rise time $\leqslant$ 200 ns Voltage 10 mV up to (for preference) 30 V Duty cycle 50 % Rise time $\leqslant$ 1 nsec.	Checking and adjusting of square-wave response of vertical channels and triggering	Generator with additional attenuator unit. Partly PG506
4. L.F. sine-wave/square-wave generator	Sine-wave: 1 Hz ... 1 MHz/0 ... 30 V Square-wave: 1 Hz ... 1 MHz/0 ... 30 V Rise time $\leqslant$ 100 ns	Checking the trigger sensitivity Checking and adjusting square-wave response of for instance attenuator unit	PM 5129
5. Cables, T-piece, terminations for the generators	General Radio types for fast rise-time square-wave and high frequency sine-wave. BNC-types for other applications.	See points 1 and 3 See points 2 and 4.	
6. Dummy probe 2 : 1	1 MΩ ± 0.1 % // 25 pF	Adjustment of input capacitance.	
7. Trimming tool kit		Adjustments	PHILIPS 800 NTX - 4822 310 50015
8. Variable mains transformer	Well-insulated output voltage 90 ... 264 Va.c.	Checking influence of mains voltage variations and adjustment of power supply.	PHILIPS ord. number 2422 529 00005
9. Moving-iron meter		Checking the power consumption of the instrument.	
10. Oscilloscope	The bandwidth must be the same or higher than the bandwidth of the instrument under test.	Various measurements.	PM 3262 PHILIPS
11. Digital multimeter	Wide voltage, current and resistance ranges. Required accuracy 0.1 %.	Checking the instrument under test.	PHILIPS PM 2527

8.1.2. Preliminary settings

- No input signals connected.
- All pushbuttons released and all switches in the CAL position.

A trace will now appear within the upper two divisions of the screen.

Clear all the four memories ACCU - STO1 - STO2 and STO3.

8.2. SURVEY OF ADJUSTING ELEMENTS AND AUXILIARY EQUIPMENT

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
POWER SUPPLY					8.3.1.
Power consumption	–	Current consumption ⩽ 300 mA at 220 V local mains	–	–	8.3.1.
+12 V supply voltage	R1646 – (A16)	+12.6 V ± 1 %	–	PM 2517 or PM 2527	8.3.1.
+5 V supply voltage	–	+5 V ± 0.25 V	–	PM 2517 or PM 2527	8.3.1.
+12 V supply voltage	–	Vary mains voltage between 200 V and 265 V. Check +12 V output (+ or – 60 mV).	–	PM 2517 or PM 2527	8.3.1.
Oscillator frequency	R1647 – (A16)	Set mains voltage to 180 V. Check +12 V output for ripple ⩽ 10 mV.	–	PM 3262	8.3.1.
C.R.T. CIRCUIT					8.3.2.
Cathode voltage	R1591 – (A15)	–1.5 V on test point X1502	–	PM 2517 or PM 2527	8.3.2.
Intensity	R1589 – (A15)	Trace just not visible	–	–	8.3.2.
Focus and Astigmatism	R1588 – (A15)	in its mid position	Sine-wave signal of 240 mVp-p – 2 kHz to X4	PM 5129	8.3.2.
	R1506 – (A15)	Sharp and well-defined trace	–	–	8.3.2.
	R1587 – (A15)	Sharp and well-defined trace	–	–	8.3.2.
Trace rotation	R16 – (front)	Horizontal trace	–	–	8.3.2.
PRE ADJUSTMENT P²CCD CIRCUIT					8.3.3.
Pre-settings	R1002 – (A10)	Set these potentiometers as indicated on unit A10		PM 2517 or PM 2527	8.3.3.
	R1006 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1007 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1008 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1024 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1026 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1027 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1080 – (A10)			PM 2517 or PM 2527	8.3.3.
	R1101 – (A11)			PM 2517 or PM 2527	8.3.3.
	R1102 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1102 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1103 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1104 – (A11)			PM 2517 or PM 2527	8.3.3.
	L1106 – (A11)			PM 2517 or PM 2527	8.3.3.
	R3057 – (A21)	Minimum trace jump when switching 0.2 ms/div to 0.5 ms/div	–	–	8.3.3.
BALANCE ADJUSTMENTS					8.3.4.
Vertical amplifier balances					8.3.4.1.
0-DC balance	CH.A – R2642 – (A21) CH.B – R2526 – (A21)	Minimum trace jump when switching 0-DC	–	–	8.3.4.1.
Attenuator balance	CH.A – R2643 – (A21) CH.B – R2527 – (A21)	Minimum trace jump when switching between 10 mV/ div – 20 mV/div – 50 mV/div	–	–	8.3.4.1.
X1/X10 balance	CH.A – R2657 – (A21) CH.B – R2534 – (A21)	Minimum trace jump when switching between 50 mV/div and 0.1 V/div	–	–	8.3.4.1.
Continue balance	CH.A – R2576 – (A21) Ch.B – R2416 – (A21)	Minimum trace shift when turning the continuous control	–	–	8.3.4.1.
Normal/Invert balance	CH.B – R2411 – (A21)	Minimum trace jump when switching Normal-Invert	–	–	8.3.4.1.
Trigger symmetry	R2819 – (A22)	Voltage on test point X2707= –1V	–	PM 2517 or PM 2527	8.3.4.2.
Trigger balances AC-DC					8.3.4.3.
External	R2753 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
A balance	R2861 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
B balance	R2859 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
LINE balance	R2857 – (A22)	No movement of trigger point when switching AC-DC	Sine-wave signal of 1,2 V p.p 2 kHz	PM 5129	8.3.4.3.
Trigger amplifier balance	R2867 – (A22)	Trigger point in middle of signal amplitude	Sine-wave signal of 1,2 V p.p 2kHz	PM 5129	8.3.4.4.

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
FINAL AMPLIFIER ADJUSTMENTS					8.3.5.
Vertical trace height	R2008 – (A20)	Display is blinking at + 4 divisions	Sine-wave signal to X3	PM 5129	8.3.5.
Display positions ACCU-ST01-ST02-ST03	R2009 – (A20)	Distance of two divisions between the traces	–	–	8.3.5.
Invert registers	–	ST01 – ST02 – ST03 are inverted	Sine-wave signal to X3	PM 5129	8.3.5.
Horizontal trace length	R2011 – (A20)	Horizontal trace length of 10 divisions	–	–	8.3.5.
Dot join adjustments	R2019 – (A20)	Equal vertical dot join faults on positive and negative going edge of the signal	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2018 – (A20)	Eliminated dot join faults	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2072 – (A20)	Dots on the screen connected with each other	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
	R2039 – (A20)	Minimum cross-talk between the channels	Sine-wave signal of 10 divisions 2 kHz	PM 5129	8.3.5.
CALibration voltage	R2017 – (A20)	3 V ± 0.7 % – 2.5 kHz	Oscilloscope and digital multimeter	PM 3262 – PM 2527	8.3.5.
VERTICAL CHANNELS					8.3.6.
Vertical amplifier sensitivity adjustments					8.3.6.1.
Channel B gain x1	R3029 – (A21)	Trace height of 6 DIV	Square-wave signal of 240 mVp-p – 2 kHz to X4	PM 5129	8.3.6.1.
Channel A gain x1	R2661 – (A21)	Trace height of 6 DIV	Square-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
Channel A gain x10	R2658 – (A21)	Trace height of 6 DIV	Square-wave signal of 24 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
Channel B gain x10	R2536 – (A21)	Trace height of 6 DIV	Square-wave signal of 24 mVp-p – 2 kHz to X4	PM 5129	8.3.6.1.
Channel A L.F. corr.	R2611 – (A21)	Straight pulse top	Square-wave signal of 240 mVp-p – 100 Hz to X3	PM 5129	8.3.6.1.
Channel B L.F. corr.	R2481 – (A21)	Straight pulse top	Square-wave signal of 240 mVp-p – 100 Hz to X4	PM 5129	8.3.6.1.
AC – DC channel A	–	Pulse top difference > 0,5 div.	Square-wave signal of	PM 5129	8.3.6.1.
AC – DC channel B	–	Pulse top difference > 0,5 div.	240 mVp-p – 100 Hz	PM 5129	8.3.6.1.
Sampling loop gain	R3009 – (A21)	Straight pulse top	Square-wave signal of 240 mV p.p – 2 kHz to X3	PM 5129	8.3.6.1.
	R 3056 – (A21)	Pulse variations are symmetrical	Square-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.6.1.
	R3057 – (A21)	Line is in middle of the screen	–	–	8.3.6.1.
IF NECESSARY PRE-ADJUST P2CCD					
Input attenuators		Straight pulse top. Pulse top errors + or –4 % maximum	Square-wave signal with a rise time ≤ 100 ns	PM 5129 2 : 1 Dummy probe 1 MHz // 25 pF	8.3.6.2.
	CH.A – CH.B	AMPL/DIV Switch / Trace-height	Amplitude and frequency		
	C2503 (C2427)	20 mV/div 6 div ± 4 %	24 mV – 2 kHz		
	C dummy	20 mV/div 6 div ± 4 %	48 mV – 10 kHz (via dummy)		
	–	0.2 V/div 6 div ± 4 %	240 mV – 2 kHz		
	–	0.2 V/div 6 div ± 4 %	480 mV – 10 kHz (via dummy)		
	C2521 (C2444)	2 V/div 6 div ± 4 %	2,4 V – 2 kHz		
	C2518 (C2442)	2 V/div 6 div ± 4 %	4.8 V – 10 kHz (via dummy)		
	C2484 (C2416)	20 V/div 6 div ± 4 %	24 V – 2 kHz		
	C2477 (C2409)	20 V/div 6 div ± 4 %	48 V – 10 kHz (via dummy)		

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
Square-wave response CH.A (CH.B), x1	R3039 - (A21) C3017 - (A21)	Pulse top errors may not exceed 1 subdivision	Square-wave signal of 1MHz - rise time ⩽ 1 ns to X3.	–	8.3.6.3.
	C2424	,,	,,	–	,,
	C2447	,,	,,	–	,,
	C2429	,,	,,	–	,,
	C2523	,,	,,	–	,,
Ch.A. square-wave response in ADD-mode	–	No change in square-wave response when operating the ADD push-button	,,	–	8.3.6.3.
CH.B. square-wave response in ADD-mode	–	No change in square-wave response when operating the ADD push-button	,,	–	8.3.6.3.
Square-wave response channel B - INVERT	–	No change in square-wave response when operating the PULL-FOR -B switch	,,	–	8.3.6.3.
Bandwidth	–	Vertical deflection must be 6 divisions at 1 MHz input and 4,6 divisions minimum at 60 MHz..	Sine-wave signal of 12 mVp-p – 60 MHz	Tektronix SG 503 + SG 504	8.3.6.4.
OFFSET control range	–	Display can be shifted more than 15 divisions on both sides	Sine-wave signal of 1.2 Vp-p – 20 MHz	Tektronix SG 503 + SG 504	8.3.6.5.
Common mode rejection	–	Rejection factor better than 100	Sine-wave signal of 960 mVp-p – 2 MHz	Tektronix SG 503 + SG 504	8.3.6.6.
TIME COEFFICIENTS					8.3.7.
Recurrent-mode	R2958 (A22)	Correct 20 ns range	Square wave signal of 160 mV-pulse repetition rate of 20 nsec to X3	Tektronix TG 501	8.3.7.1.
	R2911 (A22)	Correct start point of the trace on the screen	Square wave signal of 160 mV-pulse repetition rate of 20 ns to X3	Tektronix TG 501	8.3.7.1.
ROLL-mode	–	Correct ROLL-mode in 0.5 s/div and 1 s/div	Square wave signal with a repetition rate of 0.5 s or 1s	Tektronix TG 501	8.3.7.2.
Effective delay	–	Correct effective delay (⩾ 10 ns)	Square-wave voltage of 2.4 Vp-p – 100 kHz – rise time ⩽ 3 ns	–	8.3.7.3.
Single shot	–	Accu is refreshed	Square-wave signal of 1,2 V p.p – 1 kHz	PM 5129	8.3.7.4.
Multiple	–	All four memories are refreshed	Square-wave signal of 1,2 V p.p – 1 kHz.	PM 5129	8.3.7.5.
TRIGGERING					8.3.8.
Trigger sensitivity	R2867 – (A22)	Triggered display	Sine-wave signal of 20 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
Trigger slope and level	–	Starting point trace on positive or negative signal edge when the SLOPE switch is operated	Sine-wave signal of 240 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
	–	Correct LEVEL function	Sine-wave signal of 960 mVp-p – 2 kHz to X3	PM 5129	8.3.8.
Trigger level AUTO	–	Trigger point can be shifted over at least 4 divisions when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3	PM 5129	8.3.8.
Trigger level EXT	–	Trigger point can be shifted over total signal amplitude when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3 Sine-wave signal of 3.2 Vp-p – 2 kHz to X6	PM 5129 PM 5129	8.3.8.
Trigger level EXT÷10	–	Trigger point can be shifted over total signal amplitude when operating the LEVEL control	Sine-wave signal of 240 mVp-p – 100 Hz to X3 Sine-wave signal of 32 Vp-p – 2 kHz to X6	PM 5129 PM 5129	8.3.8.
Trigger sensitivities	–		Sine-wave signal to X3	Tektronix SG 503 + SG 504	8.3.8.
		Triggered display in AUTO	100 Hz – 0,75 div.		
		Triggered display in AUTO	60 MHz – 1,5 div.		
		Triggered display in AC	20 Hz – 0,75 div.		
		Triggered display in AC	60 MHz – 1,5 div.		
		Triggered display in DC	10 Hz – 0,75 div.		
		Triggered display in DC	60 MHz – 1,5 div		
		Triggered display in EXT	40 MHz – 0,15 V		
		Triggered display in EXT	60 MHz – 0,3 V		
		Triggered display in EXT ÷ 10	40 MHz – 1,5 V		
		Triggered display in EXT ÷ 10	60 MHz – 3 V		
	–	Triggered display in DC	Sine-wave signal of 300 mV p.p – 60 MHz to X4	Tektronix SG 503 + SG 504	8.3.8.
Triggering at mains frequency	–	Triggered display	Mains voltage derived signal of 200 mVp-p to X3	–	8.3.8.
TV triggering	–	Triggered display	T.V. signal CCIR norm – 625 lines – positive video – amplitude 0.5 division sync pulse.	–	8.3.8.
Trigger delay	R2910 – (A22)	Correct trigger delay functioning	Square-wave signal of 2 MHz – rise time ⩽ 1 ns to X3	–	8.3.8.

ADJUSTMENT	ADJUSTING ELEMENT + UNIT	ADJUSTING RESULT OR CHECK RESULT	RECOMMENDED INPUT SIGNALS	EXAMPLE OF MEASURING INSTRUMENT	CHAPTER
X-Y MODE	–	Straight line with an angle of 45° with the positive horizontal axis	Sine-wave signal of 240 mVp-p – 2 MHz to X3 and X4	–	8.3.9.
RANGE INDICATION	–	Correct V/div display change when connecting probes with range indication	–	–	8.3.10.
PLOTTER OUTPUTS	–	Correct plotting	Square-wave signal	PM 5129	8.3.11.
PERIODIC AND RANDOM DEVIATIONS	–	Ripple-noise – instability of the trace and microfony ≤ 2 mm		–	8.3.12.
EFFECT OF MAINS VOLTAGE VARIATIONS	–	No change in trace height and trace width when mains voltage is varied by + or –10 %	CAL signal to X3 and X4	–	8.3.13.

8.3. CHECKING AND ADJUSTING PROCEDURE

8.3.1. Power supply

Power consumption

- Check that the mains adapter switch S45 has been set to the local mains voltage and connect the instrument to such a voltage.
- Switch the oscilloscope on and check that the pilot lamp on POWER ON the front panel lights up.
- Check that the current consumption does not exceed 300 mA at 220 V local mains and 600 mA at 117 V local mains. (Measured with a moving-iron meter.)

+12 V supply voltage

- Check at nominal mains voltage that the voltage on the positive pole of C1513 on unit A15 is +12,6 V ± 1 %; if necessary readjust potentiometer FEEDBACK **R1646** on unit A16.
- Check that this voltage does not vary more than ± 60 mV when the mains voltage is varied between 200 V and 265 V or between 100 V and 130 V.
- Check that the +5 V on the positive pole of C1527 on unit A15 is +5 V ± 0.25 V.
- Check that the oscilloscope starts at 180 V or 90 V.

Frequency

- Set the mains input voltage to 180 V or 90 V.
- Check that the voltage on the positive pole of C1513 on unit A15 has a 100 Hz ripple that does not exceed 10 mV. If necessary; readjust potentiometer FREQ. **R1647** on unit A16.

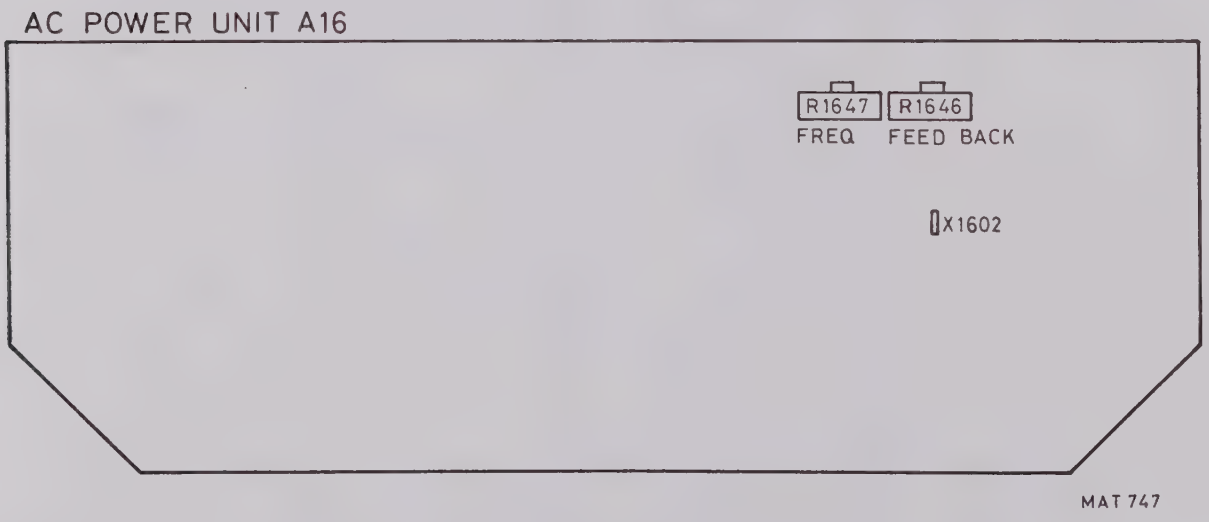


Fig. 8.3.1.

8.3.2. Cathode-ray-tube circuit

Cathode voltage

– Check that the voltage on testpoint X1502 on unit A15 is –1.5 V.
If necessary; readjust potentiometer **R1591** on unit A15.

Intensity

– Set the front panel INTENS control R15 to 90° from its left hand stop.
– Adjust potentiometer **R1589** on unit A15 in such a way that the trace is just not visible.

Focus and astigmatism

– Depress pushbutton DISPLAY STO1 S2.
– Depress pushbutton WRITE S12-A.
– Set channel A AMPL/DIV switch S20 to position 0.2 V/div. (40 mV/div. on the screen and in the alphanumeric display).
– Set TIME/DIV switch S23 to position 50 ms/div.
– Depress pushbutton AUTO S29-A of the trigger mode selector switch.
– Depress pushbutton Yx5 S16-B.
– Apply a sine-wave voltage of 240 mV-2 kHz to the A-input socket X3.
– Depress pushbutton SAVE STO1 S8.
– Depress pushbutton LOCK S12-B.
– Depress pushbutton DOTS S17.
– Set FOCUS LINE potentiometer **R1588** on unit A15 in its mid-position.
– Set the front panel INTENS control R15 to maximum brightness.
– Adjust FOCUS potentiometer **R1506** on unit A15 and ASTIGMATISM potentiometer **R1587** on unit A15 for a sharp and well-defined trace over the whole screen area.
– Check that the trace remains focused when the intensity is varied.

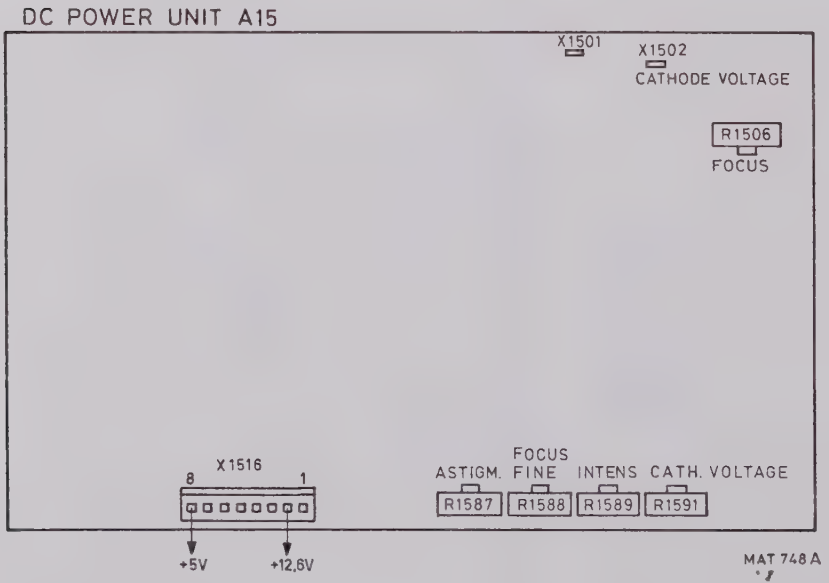


Fig. 8.3.2.

Trace rotation

– Release push-button DOTS S17.
– Depress push-button WRITE S12-A.
– Depress both push-buttons CLEAR S11 and SAVE STO1 S8 simultaneously.
– Set the STO1 Y POSITION control R4 in such a way that the trace is placed in the centre of the screen.
– Check that the trace runs exactly in parallel with the horizontal graticule lines; if necessary, readjust the TRACE ROTATION screw driver control **R16** on the front panel.
– Release push-button DISPLAY STO1 S2.
– Remove the input signal.

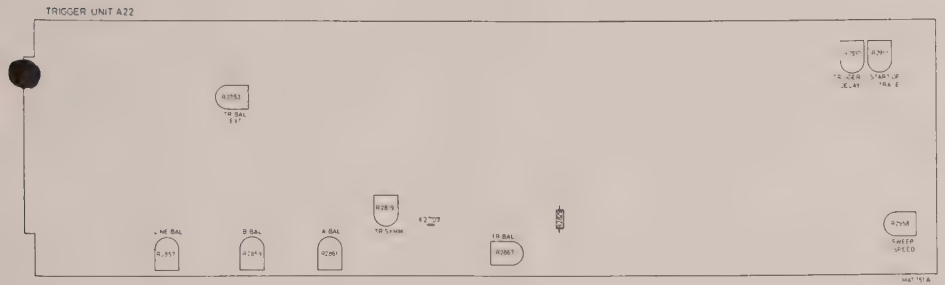


Fig. 8.3.3.

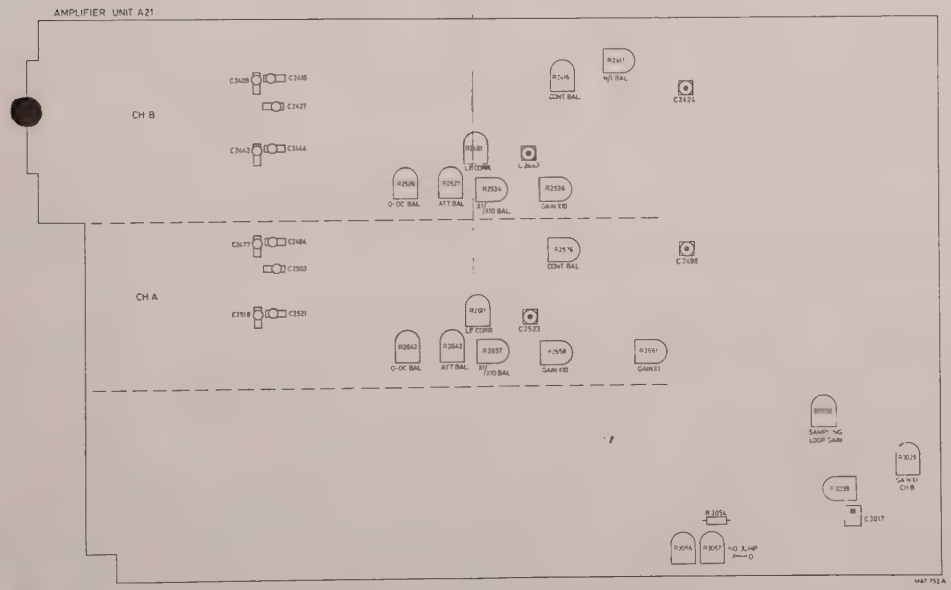


Fig. 8.3.4.

8.3.3. Pre-adjustment P²CCD circuit

– Check that the trace does not jump when the TIME/DIV switch S23 is switched between positions 0.2 ms/div and 0.5 ms/div.
If necessary, readjust potentiometer **R3057** on unit A21.

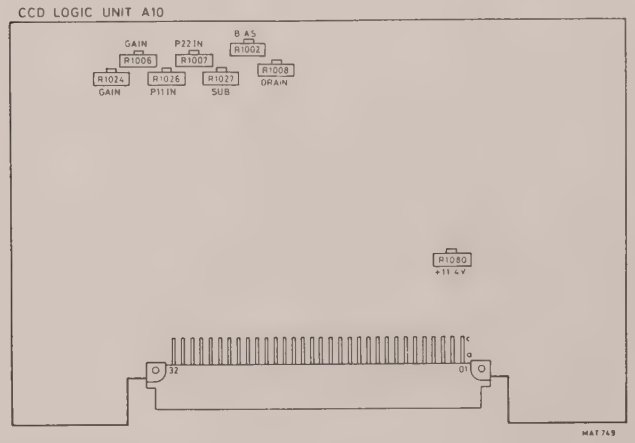


Fig. 8.3.5.

Fig. 8.3.6.

8.3.3.1. P^2CCD adjusting procedure

IMPORTANT: Before adjusting the P^2CCD be sure that the channels are adjusted correctly in direct mode.

PRELIMINARY SETTINGS

- Depress the channel A ON-OFF pushbutton S32.
- Release the channel B ON-OFF pushbutton S34.
- Set the channel A variable AMPL/DIV control R7 in the CAL position.
- Depress RECURR S38-C
- Depress pushbutton AUTO S29
- Depress pushbutton A S39
- Depress pushbutton ACCU DISPLAY S1
- Release pushbutton ST01, STO 2 and STO 3, S2, S3, S4
- Depress pushbutton WRITE S12-A
- Depress pushbutton X = T S15-A
- Depress pushbutton Y x5 S16-B
- Depress pushbutton DOTS S17
- Set the X MAGN control R2 into its CAL position.
- Depress the channel A 0 pushbutton and adjust the trace to the centre of the screen with the OFFSET control and release the 0 pushbutton.
- Set the channel A AMPL/DIV switch to .1V/DIV.
- Set the TIME/DIV switch S23 to position 0,5ms/div.

Due to the fact that the P^2CCD is divided in two parts, the following procedure is necessary to equalize the differences between these two parts.
The signal ENKEL on unit A20 must be connected to ground to obtain the possibility to use the PM 3310 oscilloscope itself for adjustings.

- Apply a sine wave of 1kHz with an amplitude to obtain 8 divisions display height to the channel A input socket X3.
- Connect point C22 of PCB connector X2003 (Unit A20) to ground.
- Set the TIME/DIV switch S23 to position 0.2ms/div.

- Connect the measuring oscilloscope to signal V OUT (testpoint X 1001 unit 10) and trigger it on the negative edge of the signal NULIN (testpoint X902 unit 9).
  Settings of the measuring oscilloscope :1V/div; 1ms/div; zero line on the centre of the screen.

ADJUSTING PROCEDURE

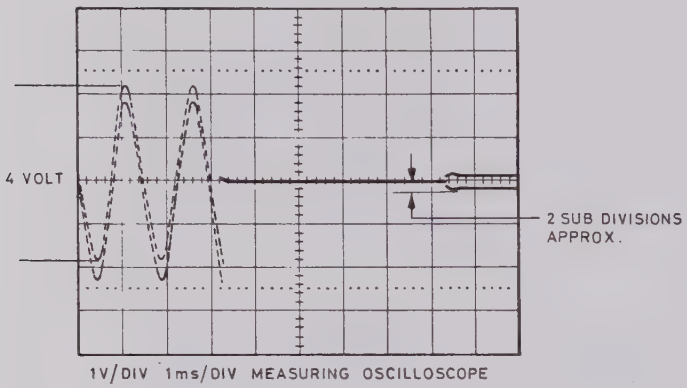
1. Adjust supply voltage at X1007-8 to 11,40 Volt with R1080.
2. Set sliders of

R 1027 to +5V	(SUB X1007-6)
R 1026 to +6V	(P11 IN X1007-4)
R 1007 to +6V	(P22 IN X1007-5)
R 1024 to midposition	
R 1006 to midposition	
R 1002 to 9V	(BIAS X1007-11)
R 1008 to 22V	(DRAIN X 1007-7)

3. Adjust **R 1101** and **R 1102** so that the signal is symmetrical aroun the zero line of the measuring oscilloscope.
4. Increase the frequency of the applied signal up to 300kHz through all time settings from 0,2ms/div. . . . . 0,5μs/div. and check that the signal remains symmetrical around the zeroline of the measuring oscilloscope. If necessary adjust **R 1007** and **R 1026** in position 0,5μs/div. Start with point 3 again and adjust for optimum and continue with point 5.
5. Apply a triangle-wave of 1kHz and set the TIME/DIV switch of the PM 3310 to 0,2ms/div. Adjust **R 1002** so that the signal on the screen of the PM 3310 cover each other. Apply a sine-wave again.
6. Set the TIME/DIV switch to 0,5ms/div and adjust the input signal to 8 divisions and switch to 0,2ms/div. again. Adjust **R 1008** so that the signals on the measuring oscilloscope cover each other within two subdivisions around the zero line (see fig. A).

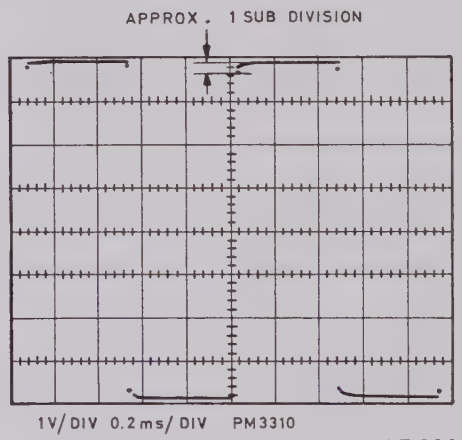
7. Adjust **R 1006** and **R 1024** for 8 divisions deflection on the screen of the PM 3310 and so that both signals cover each other. If necessary start with point 5 again.
8. Apply a square wave of 1kHz and check that the signal corresponds to fig. B. If necessary increase the SUB voltage a few volts with **R 1027**. Apply a sine wave of 1kHz again.
9. If the last adjustment was necessary start with point 3 again, and if no adjustment was made continue.
10. Increase the frequency of the applied signal to 300kHz, set the TIME/DIV switch to 0,5μs/div. and adjust **L 1102, L 1103, L 1104 and L 1106** so that the signals cover each other on PM 3310.

11. Decrease the input frequency to 1kHz and set the TIME/DIV switch to 0,2ms/div. and adjust **R 1006** and **R 1024** for 8 divisions deflection on the PM 3310 screen.
    Adjust **R 1008** so that the signals cover each other on the measuring oscilloscope within two subdivisions around the zero line (see fig. A).



MAT 907 A

Fig. A.



MAT 908 A

Fig. B.

8.3.4. Balance adjustments

The adjustments of the vertical channels A and B are identical.
The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.
These balance adjustments influence one another and must, therefore, be readjusted in the sequence in which they are described.

8.3.4.1. Vertical amplifier balances

0-DC balance

- Set channel A (B) AMPL/DIV switch S20 (S22) in position 50 mV/div.
- Check that the trace does not jump when pushbutton 0 S31 (S35) is operated.
  If necessary, readjust potentiometer **R2642 (R2526)** on unit A21 for minimum jump.
- Release the channel A (B) 0 pushbutton S31 (S35).

Attenuator balance

- Set the trace in the centre of the screen with the channel A (B) OFFSET control R10 (R12).
- Release pushbutton DOTS 16-C.
- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Check that the trace does not jump when the AMPL/DIV switch S20 (S22) is switched between 10 mV/div. 20 mV/div and 50 mV/div.
  If necessary readjust potentiometer **R2643 (R2527)** on unit A21 for minimum jump.

X1/X10 balance

- Check that the trace does not jump, when the channel A (B) AMPL/DIV switch S20 (S22) is switched between positions 50 mV/div and 0.1 V/div.
  If necessary, readjust potentiometer **R2657 (R2534)** on unit A21 for minimum jump.

Continue balance

- Set channel A (B) AMPL/DIV switch S20 (S22) in position 50 mV/div.
- Check that the trace does not move when the channel A (B) AMPL/DIV continuous control R7 (R8) is rotated between minimum and maximum.
  If necessary, readjust potentiometer **R2576 (R2416)** on unit A21 for minimum shift.
- Release the channel A (B) ON-OFF pushbutton S32 (S34) to OFF.

Follow the same procedure for channel B.

Normal/Invert balance (ONLY for channel B)

- Depress channel B ON-OFF pushbutton S34 to ON.
- Check that the trace does not jump when the channel B OFFSET control S28 is pulled and pushed.
  If necessary, readjust potentiometer **R2411** on unit A21 for minimum jump.
- Push channel B OFFSET control S28 to normal.

8.3.4.2. Trigger point symmetry

- Check that the voltage on testpoint X2707 is −1 V.
- If necessary, readjust potentiometer R2819 on the trigger-unit.

8.3.4.3. Trigger balances AC-DC

External

- Depress channel B ON-OFF pushbutton S34 to ON.
- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Set the channel B AMPL/DIV switch S22 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton EXT S39-C of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel B input socket X4 as well as to the EXT input socket X6.
- Set the LEVEL control R9 for a stable display.

- Check that the trigger point does not shift when the trigger mode selector switch S29 is switched between AC and DC. If necessary, readjust potentiometer **R2753**, on unit A22 for minimum shift, in DC-mode.
- Remove the input signal from EXT input socket X6 and from channel B input socket **X4**.

A balance

- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Set the channel A AMPL/DIV switch S20 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton A S39-A of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel A input socket X3.
- Set the LEVEL control R9 for a triggered display.
- Check that the trigger point does not move when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary, readjust potentiometer **R2861** on unit A22, in DC-mode.
- Remove the input signal from channel A input socket A3.

B balance

- Depress channel B ON-OFF pushbutton S34 to ON.
- Release channel A ON-OFF pushbutton S32 to OFF.
- Set the channel B AMPL/DIV switch S22 to position 1 V/div (0.2 V/div on the screen and in the alphanumeric display).
- Depress pushbutton B S39-B of the trigger source selector switch.
- Depress pushbutton AC S29-B of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel B input socket X4.
- Set the LEVEL control R9 for a triggered display.
- Check that the trigger point does not shift when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary, readjust potentiometer **R2859** on unit A22, in DC - mode.
- Release the channel B ON-OFF pushbutton S34 to OFF.
- Remove the input signal from channel B input socket X4.

LINE balance

- Depress pushbuttons EXT and EXT÷10 of the trigger source selector switch S39 simultaneously (LINE).
- Depress the channel A ON-OFF switch S32 to ON.
- Set TIME/DIV switch S23 to position 10 ms/div.
- Apply a mains voltage derived signal via a mains transformer with an amplitude of 6 divisions to the channel A input socket X3.
- Check that the trigger point does not move when the trigger mode selector switch S29 is switched between AC and DC.
  If necessary readjust potentiometer **R2857** on unit A22, in DC-mode.
- Remove the input signal from channel A input socket X3.

8.3.4.4. Trigger amplifier balance

- Set TIME/DIV switch S23 to position 0.5 ms/div.
- Set the LEVEL control R9 in its mid-position.
- Depress pushbutton A S39-A of the trigger source selector switch.
- Depress pushbutton AUTO S29-C of the trigger mode selector switch.
- Apply a sine-wave signal of 1.2 Vp-p – 2 kHz to the channel A input socket X3.
- Check that the trigger point is situated in the middle of the signal amplitude.
  If necessary, readjust potentiometer **R2867** on unit A22.

8.3.4.5. Trigger point symmetry

- Depress pushbutton DCS29-A of the trigger mode selector switch.
- Set LEVEL control R9 in its mid-position.
- Check that the trigger point is situated in the middle of the signal amplitude.
  If necessary, readjust potentiometer **R 2819** on unit A22.
- Remove the input signal from channel A input socket X3.

8.3.5. Final amplifier adjustments

Vertical trace height

- Depress the channel A ON-OFF switch S32 to ON.
- Depress pushbutton A of the trigger source selector switch S39.
- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Depress pushbutton Yx5 S16-B.
- Depress pushbutton WRITE S12-A.
- Depress the ACCU DISPLAY pushbutton S1.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.
- Depress pushbutton CLEAR S11 and shift the trace to −1 div simultaneously.
- Apply a signal to channel A input socket X3 with an amplitude so high that the display on the C.R.T. screen is blinking at the upper side.
- Adjust potentiometer **R2008** on unit A20 so that the display is blinking at + 4 divisions.
  If necessary, repeat this procedure.
- Remove the input signal.

Display positions ACCU - STO1 - STO2 - STO3

- Depress the four ACCU - STO1 - STO2 and STO3 DISPLAY pushbuttons S1-S2-S3 and S4.
- Depress pushbutton CLEAR S11, keep it in the depressed position and depress then the pushbuttons SAVE STO1 S8, SAVE STO2 S9, SAVE STO3 S10 and LOCK S12-B
- Turn the ACCU - STO1 - STO2 and STO3 Y POSITION controls R1-R4-R5 and R6 such that the four traces cover each other in the centre of the screen.
- Depress pushbutton Yx1 S16-A.
- Adjust potentiometer **R2009** on unit A20 for a distance of two divisions between the traces.

Invert registers

- Depress pushbutton WRITE S12-A
- Set the channel A AMPL/DIV switch S20 to position 1 V/div
- Apply a sine-wave voltage of 1.2 Vp-p – 2 kHz to the channel A input socket X3.
- Depress pushbuttons SAVE STO1 S8, SAVE STO2 S9 and SAVE STO3 S10.
- Pull the invert switches S5, S6 and S7 and check that STO1, STO2 and STO3 are inverted.
- Push the switches S5, S6 and S7.
- Remove the input signal.

Horizontal trace length

- Clear STO1, STO2 and STO3.
- Adjust with potentiometer **R2011** on unit A20 the length of the horizontal lines on the screen for 10 divisions.

Dot joint adjustments

- Release pushbutton DOTS S17.
- Depress the channel A ON-OFF pushbutton S32 to ON.
- Release the channel B ON-OFF pushbutton S34 to OFF.
- Depress pushbutton WRITE S12-A.
- Depress pushbutton Yx5 S16-B.
- Apply a sine-wave signal with a trace height for 6 divisions display and a frequency of 2 kHz to the channel A input socket X3.
- Set TIME/DIV switch S23 to position 0.2 ms/div.
- Depress pushbutton SAVE STO1 S8.
- Depress DISPLAY pushbutton STO1 S2.
- Release the ACCU - STO2 and STO3 DISPLAY buttons S1 - S3 and S4.
- Check that the dot join faults in vertical direction are equal for the positive going edge and the negative going edge of the signal.
  If necessary equalize these faults with potentiometer **R2019** on unit A20.
- Eliminate the dot join faults by adjusting potentiometer **R2018** on unit A20.
- Adjust potentiometer **R2072** on unit A20 so that the dots on the screen are really connected with each other.
- Depress the channel B ON-OFF pushbutton S34 to ON.

– Depress pushbutton SAVE STO1 S8.
– Check that in double channel operation the dot join system still functions correctly.
– Adjust potentiometer **R2039** on unit A20 for minimum cross-talk between the two channels A and B.
– Remove the input signal.
– Release pushbutton STO1 DISPLAY S2.

CALibration voltage

– Check that the amplitude of the CAL voltage on CAL terminal **X1** is 3V ± 0.7%.
  If necessary, readjust potentiometer **R2017** on unit A20.
– Check that the frequency of the CAL voltage is 2.5 kHz.

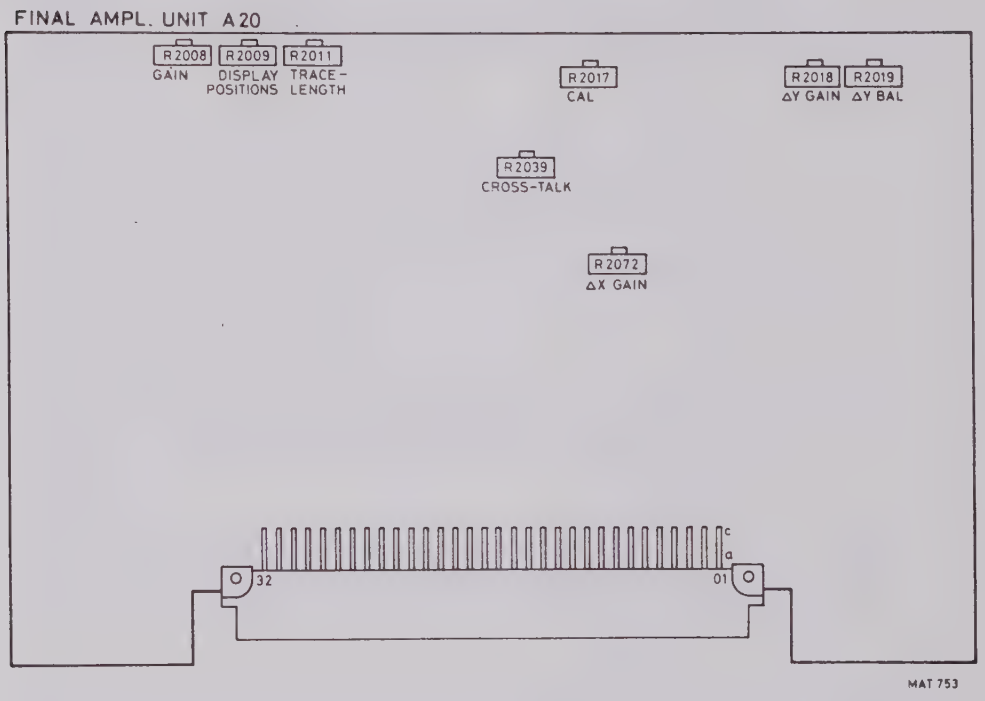


Fig. 8.3.7.

8.3.6. Vertical channels

The adjustments of the vertical channels A and B are identical.
The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

8.3.6.1. Vertical amplifier sensitivity adjustments

Before checking the sensitivities, check the balances in accordance with section 8.3.4.

Channel B gain x1

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Release the channel A and B AC-DC switches S30 and S36 and the 0 switches S31 and S35.
- Set the channel A and B AMPL/DIV switches S20 and S22 to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Set the channel A and B AMPL/DIV continuous control R7 and R8 in the CAL position.
- Set the channel A and B OFFSET controls R10 and R12 so that the traces are shifted to the centre of the screen.
- Depress pushbutton RECURR S38-C.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.
- Depress pushbutton AUTO of the trigger mode selector switch S29.
- Depress pushbutton B of the trigger source selector switch S39.
- Depress the ACCU DISPLAY pushbutton S1.
- Release the DISPLAY pushbuttons STO1 - STO2 and STO3, S2-S3 and S4.
- Depress pushbutton WRITE S12-A.
- Depress pushbutton X = t S15-A.
- Depress pushbutton Y x 5 S16-B.
- Set the XMAGN control R2 to its CAL position.
- Apply a square-wave signal of 240 mVp-p – 2 kHz to the channel B input socket X4.
- Adjust potentiometer **R3029** on unit A21 for a trace height of 6 divisions.

Channel A gain x1

- Depress pushbutton A of trigger source selector switch S39.
- Apply a square-wave signal of 240 mVp-p – 2 kHz to the channel A input socket X3.
- Adjust potentiometer **R2661** on unit A21 for a trace height of 6 divisions.

Channel A (B) gain x10

- Set channel A (B) AMPL/DIV switch S20 (S22) to position 20 mV/div (4 mV/div on the screen and in the alphanumeric display).
- Apply a square-wave signal of 24 mVp-p – 2 kHz to channel A (B) input X3 (X4).
- Adjust potentiometer **R2658 (R2536)** on unit A21 for a trace height of 6 divisions.

L.F. Correction

- Set channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Apply a square-wave signal of 240 mVp-p – 100 Hz to channel A (B) input socket X3 (X4).
- Set TIME/DIV switch S23 to position 1 ms/div.
- Check that the pulse top is straight; if necessary, readjust potentiometer **R2611 (R2481)** on unit A21.

AC-DC channel A (B)

- Depress push-button AC-DC of channel A (B) - S30 (S36).
- Check that the pulse top difference is more than 0.5 div.

Sampling loop gain

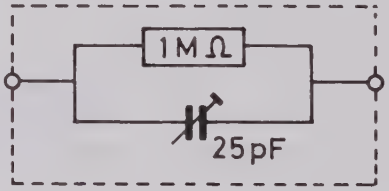
- Set the TIME/DIV switch S23 to position 0.2 ms/div.
- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Apply a square-wave signal of 240 mV – 2 kHz to channel A input socket X3.
- Set the channel B OFFSET control R12 so that the trace is set in the middle of the screen.
- Set the TIME/DIV switch S23 to position 0.5 ms/div.

– Adjust potentiometer R3009 on unit A21 so that the pulse top is straight.
– Adjust potentiometer R3056 on unit A21 so that the pulse variation is symmetrical.
– Adjust potentiometer R3057 on unit A21 so that the channel B line is in the middle of the screen.
If the range of R3057 is too small, change resistor R3054 (limits between 5K62 and 2K49).
– If necessary, repeat this procedure.

8.3.6.2. Input attenuators (square-wave response and input capacitance)

– Set TIME/DIV switch S23 to position 20 µs/div.
– Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
– Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
– Release the channel A (B) AC-DC pushbutton S30 (S36) to DC.
– Release the channel A (B) 0 pushbutton S31 (S35).
– Apply a square-wave voltage with a frequency as indicated in the table below, rise time ⩽ 100 ns to the channel A (B) input socket X3 (X4); peak to peak value as indicated in the table below.
– Check that the pulse top is straight, and pulse top errors does not exceed + or – 4%; if necessary readjust the relevant trimmers on unit A21.

2 : 1 DUMMY PROBE
1 MHz//25 pF



A (B) AMPL/DIV S20 (S22)	CHANNEL A (B) INPUT SIGNAL	ADJUSTER	TRACE HEIGHT
20 mV/div	2 kHz – 24 V	**C2503 (C2427)**	6 div +/–4 %
20 mV/div	10 kHz – 48 mV via dummy	C dummy	6 div +/–4 %
0.2 V/div	2 kHz – 240 mV	–	6 div +/–4 %
0.2 V/div	10 kHz – 480 mV via dummy	–	6 div +/–4 %
2 V/div	2 kHz – 2.4 V	**C2521 (C2444)**	6 div +/–4 %
2 V/div	10 kHz – 4.8 V via dummy	**C2518 (C2442)**	6 div +/–4 %
20 V/div	2 kHz – 24 V	**C2484 (C2416)**	6 div +/–4 %
20 V/div	10 kHz – 48 V via dummy	**C2477 (C2409)**	6 div +/–4 %

Note: The difference in input capacitance between channel A and channel B may not exceed 0.5 pF.

– Check that the range of the continuous control R7 (R8) is 1 : > 2.6.
– Remove the input signal.

8.3.6.3. Square-wave response vertical channel

Square-wave response channel A (B) x 1

– Set TIME/DIV switch S23 to position 20 ns/div.
– Depress channel A (B) ON-OFF switch S32 (S34) to ON.
– Release channel B (A) ON-OFF switch S34 (S32) to OFF.
– Set the channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
– Apply a square wave voltage of 240 mV - 1 MHz, risetime ⩽ 1 ns to the channel A (B) input socket X3.
– Check the square wave response of channel A.
Pulse top errors may not exceed 1 subdivision; if necessary, readjust R3039, C3017, C2447 and C2424, or check the square wave response of channel (B).
Pulse top errors may not exceed 1 subdivision; if necessary, readjust C2424 and C2447 (C2496 and C2523).

Channel A square-wave response in ADD-mode

- Depress pushbutton ADD S33.
- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Depress pushbutton A of the trigger source selector S39.
- Check that the square-wave response does not change when pushbutton ADD S33 is operated.

Channel B square-wave response in ADD-mode

- Release channel A ON-OFF pushbutton S32 to OFF.
- Depress channel B ON-OFF pushbutton S34 to ON.
- Depress pushbutton B of the trigger source selector S39.
- Check that the square-wave response does not change when pushbutton ADD S33 is operated.

Square-wave response channel B-INVERT

- Depress channel B ON-OFF pushbuttons S34 to ON.
- Check that the square-wave response does not change when the PULL FOR −B switch S28 is operated.
- Remove the input signal.

8.3.6.4. Bandwidth

- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Set the channel A (B) AMPL/DIV switch S20 (S22) to position 10 mV/div (2 mV/div on the screen and in the alphanumeric display).
- Apply a sine-wave signal of 12 mVp-p and a frequency of 1 MHz to channel A (B) input socket X3 (X4).
- Set TIME/DIV switch S23 in such a position that about ten sine-waves are displayed on the screen (1 ms/div).
- Check that the trace height is 6 divisions.
- Increase the frequency of the input signal to 60 MHz (amplitude still 12 mVp-p).
- Set TIME/DIV switch S23 in such a position that about ten sine-waves are displayed on the screen (20 ns/div).
- Check that during the frequency range the trace height is at least 4,6 divisions.
- Remove the input signal.

If the trace height is less than 4,6 divisions, check the square-wave response again.

8.3.6.5. OFFSET control range

- Set TIME/DIV switch S23 to position 0.2 μs/div.
- Set channel A (B) AMPL/DIV switch S20 (S22) to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Apply a sine-wave signal of 1,2 Vp-p and a frequency of 2 MHz (= 30 div).
- Check that the display can be shifted more than 15 divisions on both sides by turning the channel A (B) OFFSET controls R10 (R12).
- Remove the input signal.

8.3.6.6. Common mode rejection

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Depress the channel A and B 0 pushbuttons S31 and S35.
- Set the channel A and channel B AMPL/DIV switches S20 and S22 to positions 0.2 V/div.
- Set the channel A and channel B AMPL/DIV continuous controls R7 and R8 to their CAL positions.
- Set the channel A and B OFFSET controls R10 and R12 so that the traces are situated in the centre of the screen.
- Release the channel A and B 0 pushbuttons S31 and S35.
- Depress pushbutton ADD S33.
- Pull PULL FOR −B switch S28.
- Apply a sine-wave signal with an amplitude of 960 mVp-p and a frequency of 2 MHz to the channel A as well as the channel B input sockets X3 and X4.
- Check that the rejection factor is better than 100. (Signal < 0.25 divisions).

8.3.7. Time coefficient adjustments

8.3.7.1. Recurrent-mode

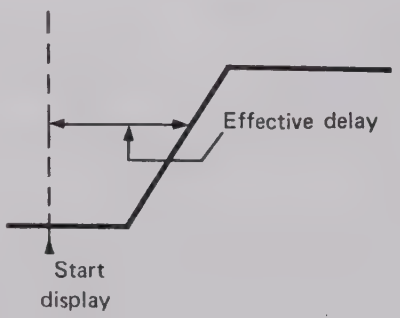
- Depress channel A ON-OFF pushbutton S32 to ON.
- Release channel B ON-OFF pushbutton S34 to OFF.
- Turn the XMAGN control R2 in the CAL position.
- Set channel A AMPL/DIV switch S20 to position 0.2 V/div (40 mV/div on the screen and in the alphanumeric display).
- Set the TIME/DIV switch S23 to position 20 ns/div.
- Apply a time marker signal of 160 mV and a pulse repetition rate of 20 ns to the channel A input socket X3.
- Check that the entre 8 cycles have a total width of 8 divisions.
  If necessary readjust potentiometer **R2958** on unit A22.
- Check that the range of the variable X-magn. R2 is 1 : > 2.5.
- Depress pushbutton DOTS S16-C.
- Turn potentiometer R2911 clockwise so that a horizontal trace appears at the left-hand side of the screen.
- Now adjust **R2911** on unit A22 so that the horizontal trace just disappears i.e. the first dot of the signal starts on the most left graticule line.
- Release pushbutton DOTS S16-C.
- Check all the TIME/DIV switch S23 positions in recurrent mode.
- Remove the input signal.

8.3.7.2. Roll-mode

- Depress pushbutton Y x 1 S16-A.
- Depress pushbutton ROLL S38-A.
- Apply a square wave signal with a repetition rate of 0.5 s to the channel A input socket X3.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 0.5 s/div.
- Depress pushbutton CLEAR S11.
- Apply a voltage of +3 V to the external socket X6 and check that the ROLL-mode starts.
- Remove the voltage from X6.
- Depress pushbutton CLEAR S11.
- Apply a square wave signal with a repretition rate of 1 s to the channel A input socket X3.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 1 s/div.
- Depress pushbutton CLEAR S11.
- Set the jumper S1201 on unit A12 in the left position.
- Depress pushbutton RUN-STOP S37.
- Check the ROLL-mode in TIME/DIV switch S23 position 60 min/div.
- Set the jumper S1201 on unit A12 in the correct position.
- Remove the input signal.

8.3.7.3. Effective delay

- Depress pushbutton RECURR S38-C.
- Depress pushbutton Yx5 S16-B.
- Set the TIME/DIV switch S23 to position 10 ns/div.
- Set channel A AMPL/DIV switch S20 to position 2 V/div (0.4mV/div. on the screen and in the alphanumeric display). Set the DELAY to 0000.
- Apply a square-wave voltage of about 2.4 Vp-p – 100 kHz and a rise time ⩽ 3 ns to the A input socket X3.
- Depress pushbutton DC of the trigger mode selector switch S29.
- Set LEVEL control R9 for a triggered display.
- Check that the effective delay is more than 1 division.



– Check the trigger sensitivity in accordance with the table below.

TRIGGER MODE	INPUT FREQUENCY	AMPLITUDE
AUTO	100 Hz	0.75 div
	60 MHz	1.5 div
AC	20 Hz	0.75 div
	60 MHz	1.5 div
DC	10 Hz	0.75 div
	60 MHz	1.5 div
EXT	40 MHz	0.15 V
	60 MHz	0.3 V
EXT ÷ 10	40 MHz	1.5 V
	60 MHz	3 V

– Check the trigger sensitivity for EXT and EXT÷10 for l.f. and h.f. signals.
– Remove the input signal.
– Depress channel B ON-OFF pushbutton S34 to ON.
– Release channel A ON-OFF pushbutton S32 to OFF.
– Set channel B AMPL/DIV switch S22 to 0.2 V/div. (40 mV/div on the screen and in the alphanumeric display).
– Depress pushbutton B of the trigger source selector switch S39.
– Apply a sine-wave signal with an amplitude of 1,5 division – 60 MHz to the channel B input socket X4.
– Check that a triggered display is obtained.
– Remove the input signal.

Triggering at mains frequency

– Depress channel A ON-OFF pushbutton S32 to ON.
– Release channel B ON-OFF pushbutton S34 to OFF.
– Depress pushbutton AC of the trigger mode selector switch S29.
– Set TIME/DIV switch S23 to position 2 ms/div.
– Depress pushbuttons EXT and EXT÷10 of trigger source selector switch S39 simultaneously (LINE).
– Apply a mains voltage derived signal of 200 mVp-p via a transformer to the channel A input socket X3.
– Check that independent on the position of LEVEL control R9 a triggered display can be obtained.
– Remove the input signal.

T.V. triggering

– Depress pushbutton A of the trigger source selector switch S39.
– Depress pushbutton TVF of trigger mode selector switch S29.
– Apply a TV signal (CCIR norm - 625 lines - positive video - amplitude 0.5 division sync. pulse) to channel A input socket X3.
– Set TIME/DIV switch S23 to position 0.1 ms/div.
– Check that a triggered display is obtained with a frame pulse and an equalization pulse on the screen.
– Remove the TV signal.

Trigger delay adjustment

– Depress pushbutton AUTO of the trigger mode selector switch S29.
– Set TIME/DIV switch S23 to 10 ns/div.
– Set the TRIGGER DELAY alphanumeric display B21 to zero by pressing both pushbuttons UP and DIGIT S24 and S25 simultaneously (RESET).
– Apply a square-wave signal of 2 MHz, rise time $\leqslant$ 1 ns to channel A input socket X3.
– Check that the leading edge of the signal is visible on the screen.
– Set the number 100 in the alphanumeric display B21 with pushbuttons DIGIT and UP S25 and S24.
– Adjust potentiometer **R2910** on unit A22 so that the leading edge of the signal is again visible on the screen.
– Set the number 0 in the display B21 by pressing both pushbuttons UP and DIGIT S24 and S25 simultaneously.
– Remove the input signal.

Trigger delay

- Set TIME/DIV switch S23 to position 0.2 ms/div.
- Depress pushbutton DC of the trigger mode selector switch S29.
- Set the number 0002 in the alphanumeric display B21 with pushbuttons DIGIT and UP S25 and S24 and set pushbutton DIGIT S25 to the least significant DIGIT (= 2).
- Apply a square-wave voltage of 2 kHz to the channel A input socket X3.
- Set LEVEL control R9 for a triggered display.
- Set TIME/DIV switch S23 step by step to position 0,5 μs/div. and check at each position that the beginning of the signal can be shifted in the screen by using pushbutton UP S24.
- Set the TIME/DIV switch S23 to position 0.2 μs/div and check that the number in the alphanumeric display B21 is 100 (max. value in sampling mode-"repetitive only").

8.3.9. X-Y mode

- Depress the channel A and B ON-OFF pushbuttons S32 and S34 to ON.
- Depress the channel A and B pushbuttons "0" S31 and S35.
- Set the channel A and B AMPL/DIV switch S20 and S22 to 0.2 V/div.
- Set TIME/DIV switch S23 to position 0.5 μs/div.
- Set the channel A and B OFFSET controls R10 and R12 so that the spot is shifted to the centre of the screen.
- Release the channel A and B pushbuttons "0" S31 and S35.
- Depress pushbutton X = A/Y = B S15-B.
- Apply a sinewave signal of 240 mVp-p – 2 MHz to the channel A as well as the channel B input sockets X3 and X4.
- Check that a straight line is displayed with a angle of 45° with the positive horizontal axis.
- Check the same with TIME/DIV switch S23 in position 0.2 μs/div.
- Depress the channel A "0" pushbutton S31.
- Check that a vertical line is displayed.
- Remove the input signals.

8.3.10. Range indication

- Depress pushbutton X = t S15-A.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Release channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Read the A (B) V/div. alphanumeric display B10 (B11) contents.
- Connect a probe with range indication to the channel A (B) input socket X3 (X4).
- Check that the indication in the A (B) V/div. alphanumeric display B10 (B11) is changed by a factor of 10.

8.3.11. Plotter outputs

- Store a square-wave signal of 1 div. in memory STO1.
- Select memory STO1 with SELECT pushbutton S14.
- Connect voltmeters to the plotter output sockets on the rear side of the instrument.
- Depress pushbutton PLOT S18 and check the following:
  1. X-OUT and Y-OUT are 0 Volt
  2. PENLIFT goes to 0 Volt
  3. X-OUT and Y-OUT are generating output signals
- Check that during plotting an intensified dot is visible on the screen.
- Depress pushbutton PLOT S18 again and check that the PLOT action is stopped.
- Remove the input signal.

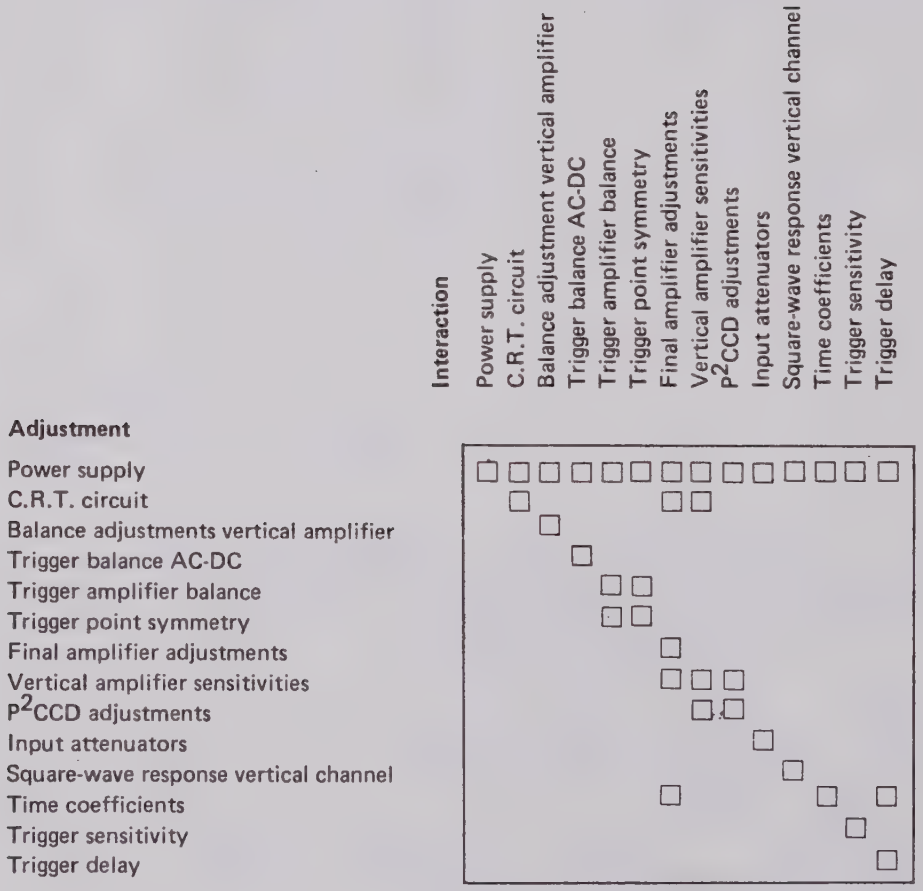
8.3.12. Periodic and random deviations

These must be checked only with the cabinet plates fitted:

- Depress pushbutton RECURR S38-C.
- Set TIME/DIV switch S23 to position 1 ms/div.
- Depress channel A (B) ON-OFF pushbutton S32 (S34) to ON.
- Depress channel B (A) ON-OFF pushbutton S34 (S32) to OFF.
- Release the channel A and B pushbuttons "0" S31 and S35.
- Depress pushbuttons AC/DC of the input coupling controls S30 and S36 to AC.
- Set both AMPL/DIV switches S20 and S22 to positions 10 mV/div and the AMPL/DIV continuous controls R7 and R8 to their CAL positions.
- Depress pushbutton AUTO of the trigger mode switch S29.
- Check that ripple-noise-instability of the trace and microfony does not exceed 4 mm.

8.3.13. Effect of mains voltage variations

- Depress channel A ON-OFF pushbutton S32 to ON.
- Depress channel B ON-OFF pushbutton S34 to ON.
- Set channel A AMPL/DIV switch S20 to position 1 V/div.
- Set channel B AMPL/DIV switch S22 to position 1 V/div.
- Connect the CAL terminal x1 output signal with the channel A as well as the channel B input sockets X3 and X4.
- Vary the mains voltage by + and –10 %.
- Check that neither trace height nor trace width changes and that the brilliance remains the same.


Interaction
Power supply
C.R.T. circuit
Balance adjustment vertical amplifier
Trigger balance AC-DC
Trigger amplifier balance
Trigger point symmetry
Final amplifier adjustments
Vertical amplifier sensitivities
P2CCD adjustments
Input attenuators
Square-wave response vertical channel
Time coefficients
Trigger sensitivity
Trigger delay
Adjustment
Power supply
C.R.T. circuit
Balance adjustments vertical amplifier
Trigger balance AC-DC
Trigger amplifier balance
Trigger point symmetry
Final amplifier adjustments
Vertical amplifier sensitivities
P2CCD adjustments
Input attenuators
Square-wave response vertical channel
Time coefficients
Trigger sensitivity
Trigger delay

8.5. PERFORMANCE CHECK

8.5.1. General information

WARNING: Before switching on, ensure that the oscilloscope has been installed in accordance with the instructions outlined in chapter 2 of the operating manual, Installation Instructions.

This procedure is intended to be used for incoming inspection to determine the acceptability of newly purchased or recently recalibrated instruments.
It does not check every facet of the instrument's calibration; rather it is concerned primarily with those portions of the instrument which are essential to measurement accuracy and correct operation. Removing the instrument covers is not necessary to perform this procedure. All checks are made from the front panel.

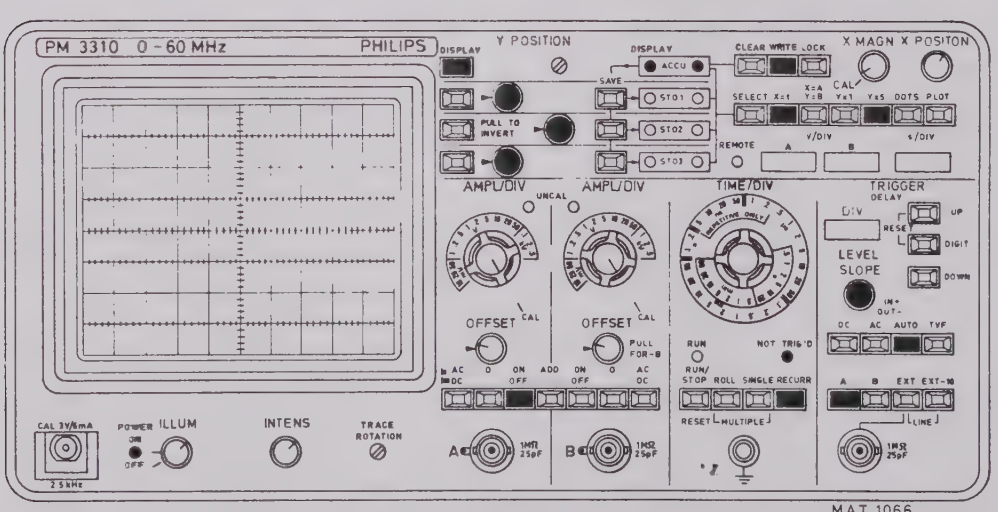
If this test is started a few minutes after switching on, bear in mind that test steps may be out of specification, due to insufficient warming-up time. To avoid this situation, allow the specified warming-up time.

The performance checks are made with a stable, well-focused, low intensity display. Unless otherwise noted, adjust the intensity and trigger-level controls as needed.

Note 1: At the start of every check, the controls always occupy the preliminary settings; unless otherwise stated.
Note 2: The input voltage has to be supplied to the A-input; unless otherwise stated.
Note 3: Set the TIME/DIV switch to a suitable position; unless otherwise stated.

8.5.2. Preliminary settings of the controls

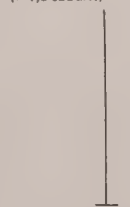
- Start this check procedure with **NO** input signals connected, **ALL** pushbuttons released and **ALL** switches in the CAL position.
- Depress the controls as indicated in figure below.

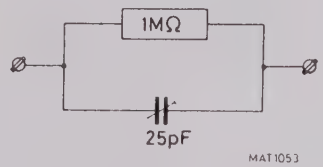


8.5.3. Recommended test equipment

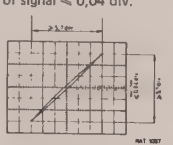
Type of instrument	*Specifications*	*Example of recommended instrument*
Constant amplitude sine-wave generator	Freq. 200kHz ... 60MHz Constant amplitude of 12mVp-p ... 1.2Vp-p	Tektronix SG503 + SG504
Time marker generator	Repetition rate 0.5s ... 20ns	Tektronix TG501
Square-wave calibration generator	Rise time $<$ 200ns Voltage 10mV up to (for preference) 30V. Duty cycle 50% Rise time $\leqslant$ 1nsec.	Generator with additional attenuator unit. Partly PG506
L.F. sine-wave/square-wave generator	Sine-wave: 1Hz ... 1MHz/0 ... 30V Square-wave: 1Hz ... 1MHz/0 ... 30V Rise time $\leqslant$ 100ns	PM5129
Cables, T-piece, terminations for the generators	General Radio types for fast rise-time square-wave and high frequency sine-wave. BNC-types for other applications.	
Dummy probe 2 : 1	1MΩ $\pm$ 0.1% // 25pF	
Variable mains transformer	Well-insulated output voltage 90 ... 264V.a.c.	PHILIPS' ord. number 2422 529 00005
Moving-iron meter		

CHECKING PROCEDURE

STEP	OBJECTIVE	INPUT VOLTAGE	SETTINGS	REQUIREMENTS	MEASURING RESULTS
A.	**POWER ON + DISPLAY**				
A.1.	Start power on		Set the power on/off switch to ON	Starts at 180 V (Q-version: at 90 V) Pilot lamp POWER ON lights up	
A.2.	Current consumption			600 mA max. at 110 V 300 mA max. at 220 V	
A.3.	Illumination Intens Focus		Illumination potentiometer Intens potentiometer Intens potentiometer	Normal brightness adjusting Normal intens adjusting Automatic focus adjusting	
A.4.	Trace rotation			Line must be in parallel with horizontal graticule lines; if necessary, readjust potentiometer TRACE ROTATION	
B.	**VERTICAL SELECTIONS**				
B.1.	Channel control A (B)		Depress pushbutton ON of ch. A (ch. B)	Trace channel A (B) is visible on the screen	
B.2.	O-DC-AC control A (B)	Sine-wave signal, 2 kHz + DC offset to ch. A (ch. B)		Adjust the sine-wave amplitude so that the trace heigh is ca. 4 div.	
			Depress pushbutton O of ch. A (ch. B)	Set the trace in the centre of the screen	
			Release pushbutton O of ch. A (ch. B)		
			Depress pushbutton AC of ch. A (ch. B)	Signal is visible on the screen, centre of the sine-wave is on the centre of the screen	
			Release pushbutton AC of ch. A (ch. B); eg. DC	Signal is visible on the screen, centre of the sine-wave is on DC-offset level.	
B.3.	ADD	Sine-wave signal, 2 kHz to ch. A and ch. B	Depress pushbutton ADD	Signal amplitude is the adding of ch. A + ch. B	
B.4.	Vertical trace height	Sine-wave signal 480 mVp-p 2 kHz	Ampl./Div. switch = 0,2 V/div.		
			Depress Display ACCU; STO 1; STO 2 and STO 3		
			Depress SAVE STO 1; STO 2 and STO 3		
			Depress pushbutton Yx1	Max. signal amplitude = 2 div. all 4 signals are blinking at upper and lower top	
B.5.	Invert stores	As B.4.	As. B.4. Pull the INVERT switches of STO1, STO 2 and STO 3	Display of STO 1, STO 2 and STO 3 is inverted	
B.6.	Dot join	As B.4.	As. B.4. Depress pushbutton DOTS	Signals are built up by dots	
C.	**VERTICAL CHANNELS**				
C.1.	Vertical gain A (B)	Square-wave signal 240 mVp-p 2 kHz to ch. A (ch. B)	AMPL/DIV switch = 0,2 V/div.		
			Depress pushbutton Yx1	Trace height = 1,2 div. ± 3% (± 0,2 subdiv.)	
			Depress pushbutton Yx5	Trace height = 6 div. ± 5% (± 1,5 subdiv.)	
C.2.	AMPL/DIV positions	Square-wave signal, freq. 2 kHz to ch. A (ch. B)	AMPL/DIV switch position:		
		Ampl: 12 mV p-p 24 ,, 60 ,, 120 ,, 240 ,, 600 ,, 1,2 Vp-p 2,4 ,, 6 ,, 12 ,, 24 ,, 60 ,,	10 mV/div. 20 ,, 50 ,, 0,1 V/div. 0,2 ,, 0,5 ,, 1 ,, 2 ,, 5 ,, 10 ,, 20 ,, 50 ,,	Trace height = 6 div. ± 5% (± 1,5 subdiv.) 	

STEP	OBJECTIVE	INPUT VOLTAGE	SETTINGS	REQUIREMENTS	MEASURING RESULTS
C.3.	Continue range A (B)	Square-wave signal 240 mV - 100 Hz to ch. A (ch. B)	Continue potentiometer ↶	Continue range 1:>2,5 Pilot lamp "UNCAL" lights up	
C.4.	Vertical deflection A (B) via dummy  	Square-wave signal, freq. 10 kHz to ch. A (ch. B)	AMPL/DIV switch position:		
		Ampl.: 48 mVp-p 480 " 4,8 Vp-p 48 "	20 mV/div. 0,2 V/div. 2 " 20 "	Trace height = 6 div. ± 5% (± 1,5 subdiv.)	
C.5.	Square-wave response (A, B and – B)	Square-wave signal, 240 mVp-p, 1 MHz, risetime ⩽ 1 nsec. to ch. A (ch. B)	AMPL/DIV switch = 0,2 V/div. (for – B: pull the PULL FOR – B switch)	Pulse abberations ± 3%, risetime ⩽ 6 nsec.	
C.6.	Visible signal delay	As C.5.	AMPL/DIV switch = 0,2 V/div. TIME/DIV switch = 10 ns/div.	Visible signal delay > 10 nsec. NOTE: remember the value for point E.7	
C.7.	Bandwidth A (B)	Sine-wave signal to ch. A (ch. B) 1 MHz		Adjust the sine-wave amplitude so that the trace height = 6 div.	
		1 MHz - 60 MHz		Trace height ⩾ 4,2 div.	
C.8.	Offset control range A (B)	Sine-wave signal 1,2 Vp-p, 2 MHz to ch. A (ch. B)	AMPL/DIV switch = 0,2 V/div. OFFSET control of ch. A (ch. B) ↶ or ↷	Sine-wave signal out of the screen	
C.9.	Common mode rejection A and – B	Sine-wave signal 960 mVp-p, 2 MHz to ch. A and ch. B	AMPL/DIV switch = 0,2 V/div. Depress push-button ADD Pull the PULL FOR – B switch	Rejection > 100 (signal < 0,25 div.)	

STEP	OBJECTIVE	INPUT VOLTAGE	SETTINGS	REQUIREMENTS	MEASURING RESULTS
D.	**TIME BASE**				
D.1.	Time coëfficients	Square wave signal to ch. A	TIME/DIV switch position:		
	– Recurrent	Repetition time:		Coëfficient error ± 2% (c.i.0,2 div. over 10 div. screenwith) (Combined with magnifier: coëfficient error ± 4%)	
		5 nsec	5 nsec/div.		
		10 nsec	10 nsec/div.		
		20 nsec	20 nsec/div.		
		50 nsec	50 nsec/div.		
		0,1 µsec	0,1 µsec/div.		
		0,2 µsec	0,2 µsec/div.		
		0,5 µsec	0,5 µsec/div.		
		1 µsec	1 µsec/div.		
		2 µsec	2 µsec/div.		
		5 µsec	5 µsec/div.		
		10 µsec	10 µsec/div.		
		20 µsec	20 µsec/div.		
		50 µsec	50 µsec/div.		
		0,1 msec	0,1 msec/div.		
		0,2 msec	0,2 msec/div.		
		0,5 msec	0,5 msec/div.		
		1 msec	1 msec/div.		
		2 msec	2 msec/div.		
		5 msec	5 msec/div.		
		10 msec	10 msec/div.		
		20 msec	20 msec/div.		
		50 msec	50 msec/div.		
		0,1 sec	0,1 s/div.		
		0,2 sec	0,2 s/div.		
	– Roll		Depress pushbutton ROLL Start every action with RUN		
		0,5 sec	0,5 s/div.	Coëfficient error ± 2% (c.i.0,2 div. over 10 div. screenwith) During action pilot lamp "RUN" lights up After action pilot lamp "RUN" flashes	
		1 sec	1 s/div.		
		2 sec	2 s/div.		
		5 sec	5 s/div.		
		10 sec	10 s/div.		
		20 sec	20 s/div.		
		0,5 min(30 sec)	0,5 min/div.		
		1 min(60 sec)	1 min/div.		
		2 min(120 sec)	2 min/div.		
		6 min(360 sec)	6 min/div.		
		15 min(900 sec)	15 min/div.		
		30 min(1800 sec)	30 min/div.		
		60 min(3600 sec)	60 min/div.		
D.2.	Variable X-magn. range	Square-wave signal, to ch. A repetition time 10 msec	TIME/DIV switch position 1 ms/div.	X-magnifier range = 1 ⩾ 2,5	
D.3.	Single shot	Square-wave signal, 1 kHz to ch. A	TIME/DIV switch position 1 ms/div. Depress pushbutton SINGLE Depress pushbutton Yx1 Start every action with RUN	ACCU is refreshed and during the single shot action the pilot lamp "NOT TRIG'D" lights up	
D.4.	Multiple	As D.3.	TIME/DIV switch position 1 ms/div. Depress pushbuttons ROLL, and SINGLE (c.i.MULTIPLE) Depress Display ACCU; STO 1; STO 2 and STO 3 Depress pushbutton Yx1 Start every action with RUN	ACCU, STO 1, STO 2 and STO 3 are refreshed and during the Multiple action the pilot lamp "NOT TRIG'D" lights up	

STEP	OBJECTIVE	INPUT VOLTAGE SETTINGS		REQUIREMENTS	MEASURING RESULTS
E.	**TRIGGERING**			*(NOTE: If signal triggers the pilot lamp "NOT TRIG'D" is extinguished)*	
E.1.	Sensitivity A (B)	Sine-wave signal to ch. A (ch. B) frequency	Depress pushbutton A (B)		
		100 Hz	Depress pushbutton AUTO	Signal triggers at 0,75 div.	
		20 Hz	Depress pushbutton AC	Signal triggers at 0,75 div.	
		10 Hz	Depress pushbutton DC	Signal triggers at 0,75 div.	
		40 MHz		Signal triggers at 0,75 div.	
		60 MHz		Signal triggers at 1,5 div.	
E.2.	Sensitivity EXT	Sine-wave signal to EXT frequentie	Depress pushbutton EXT		
		40 MHz	Depress pushbutton DC	Signal triggers at 0,15 Vp-p	
		60 MHz		Signal triggers at 0,3 Vp-p	
	EXT÷10	40 MHz	Depress pushbutton EXT÷10	Signal triggers at 1,5 Vp-p	
		60 MHz		Signal triggers at 3 Vp-p	
E.3.	Slope	Sine-wave signal 240 mVp-p, 2 kHz to ch. A	AMPL/DIV switch = 0,2 V/div.	Signal triggers on positive going edge	
			Pull the SLOPE switch	Signal triggers on negative going edge	
E.4.	Level range	As E.3.	LEVEL control	Trace is triggered in the most extreme positions of the LEVEL control	
			Depress pushbutton AC LEVEL control	Trace is not triggered in the most extreme positions of the LEVEL control	
			Depress pushbutton DC LEVEL control	Trace is not triggered in the most extreme positions of the LEVEL control	
		Increase the sine-wave signal to 1,2 Vp-p, 2 kHz	LEVEL control	Trace is triggered in the most extreme positions of the LEVEL control	
E.5.	T.V. triggering	T.V. signal according to C.C.I.R. (625 lines), ampl. sync.pulse = 0,5 div.p-p	Depress pushbutton TVF	Signal triggers	
E.6.	Display range trigger delay		If necessary, depress push-button UP, DOWN or DIGIT		
			TIME/DIV switch = 1 ms/div.	Display range is – 9 ... 9999 div.	
			TIME/DIV switch = 0,2 µs/div.	Display range is 0 ... 100 div.	
E.7.	Accuracy trigger delay	Square-wave signal, repetition time = 0,1 msec to ch. A	TIME/DIV switch = 20 µs/div. Trigger delay = 0000	Accuracy = 0	
			Trigger delay = 1900	Accuracy = ± 2 mm (1 subdiv.)	
			Trigger delay = 9999	Accuracy = 0,01% (for 9999 : 1 div.) *NOTE: Wait for a trigger pulse !*	
		Square-wave signal, repetition time = 1 µsec to ch. A	TIME/DIV switch = 0,2 µs/div. Trigger delay = 0000	Accuracy = 0	
			Trigger delay = 0100	Accuracy = ± 2 div. + visible delay (for visible delay, see point C.7.)	
F.	**X-Y Mode**	Sine-wave signal, 240 mVp-p, 2 MHz to ch. A and ch. B	Depress pushbutton ON of ch. A and ch. B Depress pushbutton X=A, Y=B Set the ch. A and ch. B AMPL/DIV switches to 0,2 V/div.	– A line is visible with an angle of 45° with the horizontal axis – Amplitude of X-defl. and Y-defl. is ⩾ 5,7 div. – Distance between lines in centre of signal ⩽ 0,04 div. 	
G.	**Plotter outputs**	Sine-wave voltage, 480 mVp-p, 2 kHz to ch. A	AMPL/DIV switch = 0,2 V/div. Depress pushbutton PLOT	– Check that the plot action starts by depressing pushbutton PLOT – Plottime ≈ 100 sec – During plot: penlift = 100 V X-out = 1 V max. Y-out = 1 V max. intensified dot is visible on the screen	
H.	**Calibration**			Calibration voltage = 3 Vp-p Calibration frequency = 2,5 kHz	

9. CORRECTIVE MAINTENANCE

9.1. REPLACEMENTS

WARNING: The opening of covers or removal of parts, except those to which access can be gained by hand, is likely to expose live parts, and also accessible terminals may be live.
The instrument shall be disconnected from all voltage sources before any adjustment, replacement or maintenance and repair during which the instrument will be opened.
If afterwards any adjustment, maintenance or repair of the opened instrument under voltage is inevitable, it shall be carried out only by a skilled person who is aware of the hazard involved.
Bear in mind that capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.

Standard parts

Electrical and mechanical replacement parts can be obtained through your local Philips organisation or representative. However, many of the standard electronic components can be obtained from other local suppliers.
Before purchasing or ordering replacement parts, check the parts list for value tolerance, rating and description.

Note: Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known that a substitute will not degrade instrument performance.

Special parts

In addition to the standard electronic components, some special components are used.
These components are manufactured or selected by Philips to meet specific performance requirements.

Transistors and integrated circuits

Transistors and I.C.'s (integrated circuits) should not be replaced unless they are actually defective. If removed from their sockets during routine maintenance return them to their original sockets. Unnecessary replacement or switching of semiconductor devices may affect the calibration of the instrument. When a transistor is replaced, check the operation of the part of the instrument that may be affected. (see interaction table 8.4.)

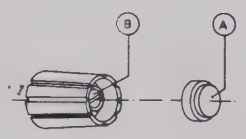
WARNING: Handle silicone grease with care. Avoid getting silicone grease in the eyes. Wash hands thoroughly after use.

Any replacement component should be of the original type or a direct replacement. Bend the leads to fit the socket and cut the leads to the same length as on the component being replaced.

9.1.1. Replacing single knobs

- Prise off cap A.
- Slacken screw (or nut) B.
- Pull the knob from the spindle.

When fitting a knob or cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.



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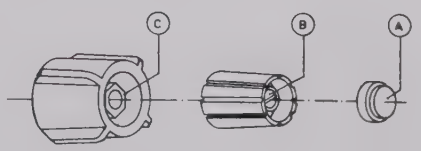
9.1.2. Replacing double knobs

- Prise off cap A and slacken screw B.
- Pull the inner knob from the spindle.
- Slacken nut C and pull the outer knob from the spindle.

When fitting a knob or cap, ensure that the spindle is in a position which allows reference lines to be coincident with the markings on the text plate of the oscilloscope.



MAT 163

9.1.3. Replacing carrying handle

1. Remove both the upper and lower cabinet plates after slackening the four quick-release fasteners at the corners of each plate. To prevent the fasteners coming apart, do not slacken more than two turns.
2. Remove the plastic strip which is snapped on to the grip.
3. Remove the four screws which secure the grip to the brackets (these screws have been locked with a sealing varnisch).
4. Depress the push-buttons in the brackets and turn the carrying handle as far as possible to the upper side of the oscilloscope.
5. Keep the push-button of the right-hand bracket depressed and pull the bracket from its bearing 1).
6. Remove the grip from the remaining bracket.
7. Depress the push-button of the left-hand bracket and turn the latter as far as possible to the lower side of the instrument.
8. Keep the push-button depressed and pull the bracket from its bearing.

If it is impossible to remove the left-hand bracket in this way, remove also its bearing in a similar way as described in footnote 1).

1) With some instruments it may be impossible to remove the handle in the described way. This is due to an extra securing plate in the right-hand bearing. In that case, DO NOT USE FORCE, but work in accordance with the following procedure which replaces points 3, 4 and 5.

3. Remove the two screws which secure the grip to the right-hand bracket.
4. Remove the two hexagonal bolts which secure the right-hand bearing to the side strip.
5. Depress the push-button of the right-hand bracket and take the bearing from the bracket.

9.1.4. Removing the cabinet plates and the screen bezel

Both upper and lower cabinet plate can be removed after slackening one or two turns the four quick release fasteners at the corners of each plate. Do not slacken the fasteners more than two turns, otherwise they may come apart.

The screen bezel can be detached by pressing the longer edges and pulling out.

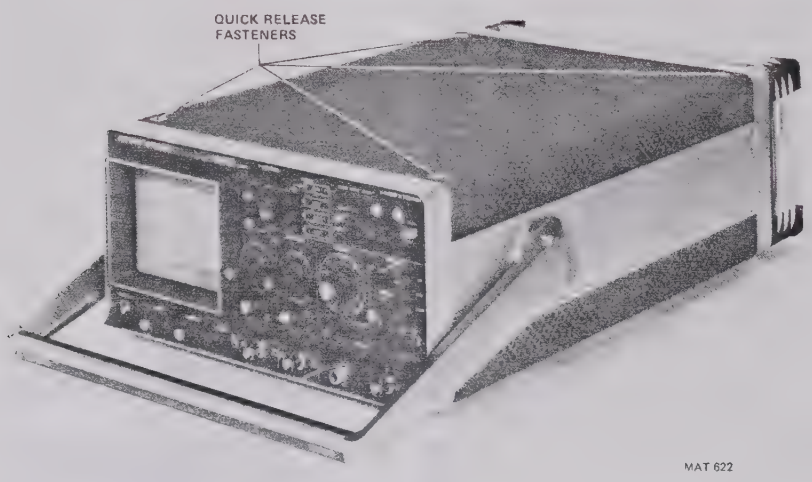


Fig. 9.1.1.

Fig. 9.1.2.

9.1.5. Replacing the plug-in units

The plug-in units are:

A4 – microprocessor unit
A6 – RAM unit
A7 – buffer unit
A8 – conversion unit
A9 – ACL unit
A10 – CCD logic unit
A12 – time-base unit
A13 – delay trigger unit
A14 – IEC bus interface (if available)
A20 – final amplifier unit

These circuit boards can be easily removed after disconnecting the various cables.
Unit A10 can only be removed after slackening the screw at the upper right side of the unit which secures the heatsinks to the metal spport.

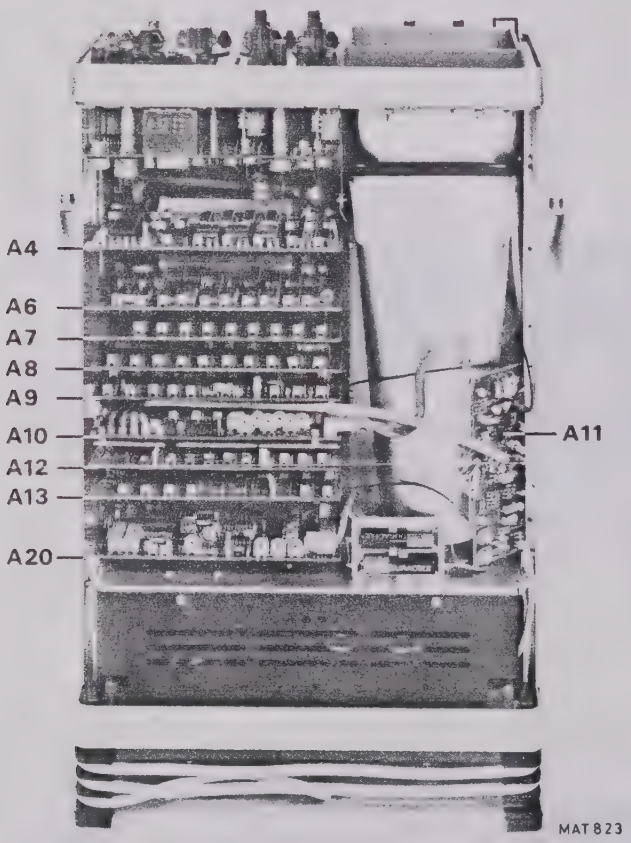


Fig. 9.1.3.

9.1.6. Replacing the P2CCD unit A11

This unit A11 is located at the upper left side of the instrument above the C.R.T.

- Remove the four miniature coaxial plugs from unit A10.
- Remove the multipole connector from unit A10.
- Remove the two miniature coaxial plugs from unit A11.
- The unit can be removed after unscrewing the two screws which secure the unit to the side frame.

ATTENTION: The P2CCD is a highly sensitive MOS circuit. Upon delivery of a spare unit the miniature coaxial plugs are interconnected so that no static charge can influence the circuit.
Moreover the multipole connector is short circuited by a conductive plastic foam material.
When mounting a new unit, first secure the unit mechanically to the side frame.
After having taken the precautions as described in chapter 9.3. remove the conductive plastic foam of the multipole connector and plug it in the CCD logic unit.
After that, the miniature coaxial connectors may be disconnected and connected to the right connectors one by one.

9.1.7. Replacing the front unit A2

- Remove the screen bezel and the contrast plate.
- Remove all the knobs except the pushbutton knobs.
- Remove the textplate with the two screws underneath the channel A AMPL/DIV switch and the TIME/DIV switch.
- Remove the four screws as indicated in the figure.

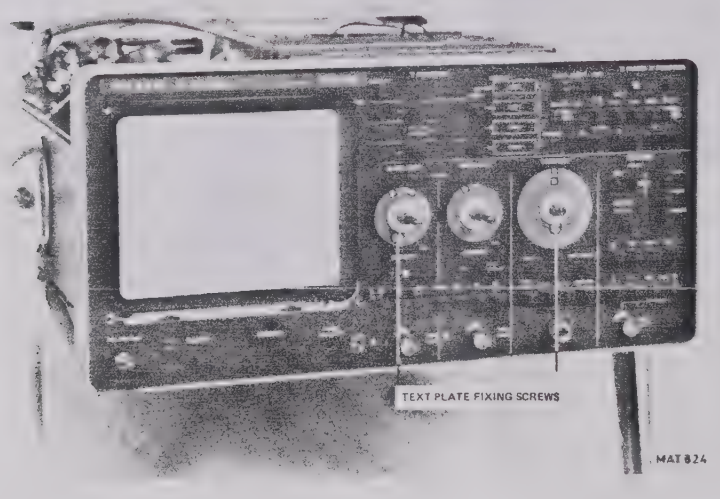


Fig. 9.1.4.

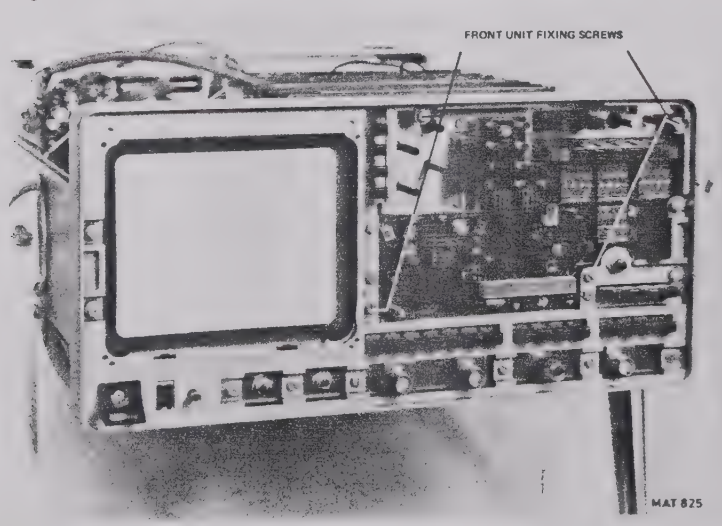


Fig. 9.1.5.

- Remove plug in unit A4.
- Disconnect the two multipole connectors on the motherboard unit A3 which are situated behind the front unit.
- Press the front unit to the rear by pushing the connector which is mounted underneath the TIME/DIV switch.
- Carefully remove the unit out of the instrument.
- When mounting again, carefully insert the front unit into the instrument.
- Be sure that the bottom of the unit is completely outlined with the connector on the motherboard.
- Carefully press the front unit into the connector.
- Fix the unit, the textplate and the knobs again in the reversed sequence.
- Plug in the microprocessor unit A4.
- Plug in the two multipole connectors.

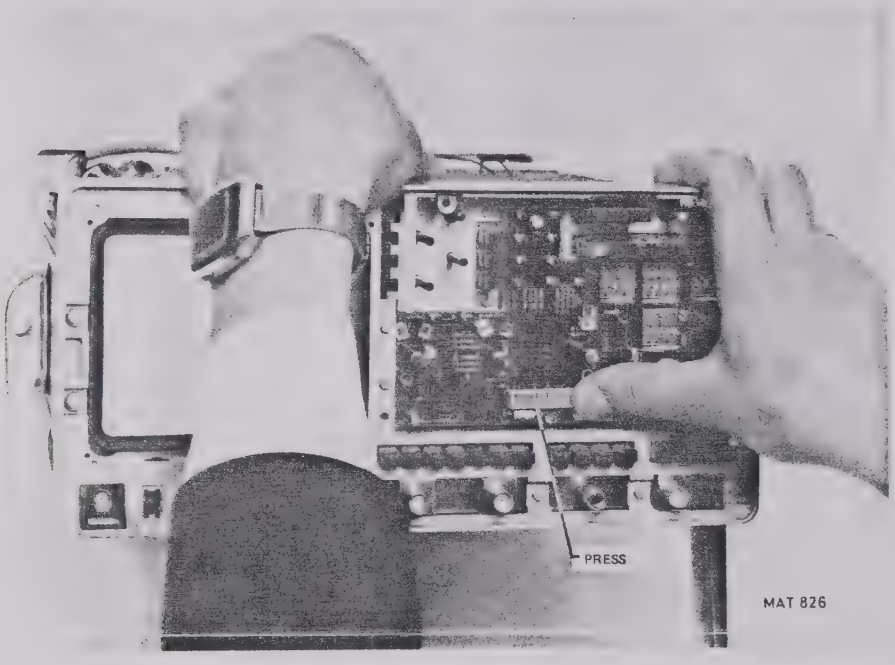


Fig. 9.1.6.

9.1.8. Replacing the LEVEL control

- Remove the front unit A2.
- Unsolder the wires on the potentiometer.
- Unscrew the potentiometer.

9.1.9. Replacing the trigger mode selector switch

- Remove the front unit A2.
- Unsolder the interconnection wire between the LEVEL potentiometer and the switch.
- Remove the two slot headed screws on the front that fixes the switch.

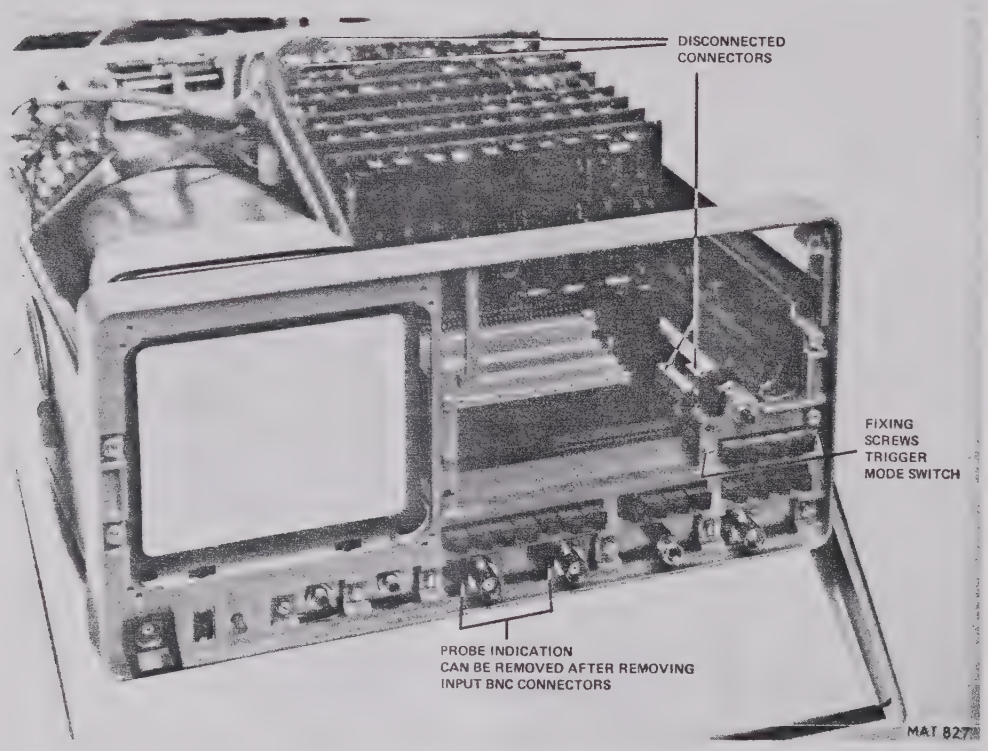


Fig. 9.1.7.

9.1.10. Replacing the C.R.T.

WARNING: Handle the C.R.T. carefully. Rough handling or scratching can cause the C.R.T. to implode.

- Remove the upper and lower instrument cabinet plate.
- Remove the bezel and the contrast plate.
- Remove the two screws that secure the upper scale illumination lamps support to the front panel and remove this support.
- Disconnect the two connectors on the C.R.T. socket from the power supply unit (A15) and the final amplifier unit (A20).
- Unsolder the red and yellow TRACE ROTATION wire from the support in the front underneath the C.R.T.
- Loosen the screw of the clamping bracket around the C.R.T. neck (accessible via the hole in the C.R.T. screen).
- Carefully withdraw the C.R.T. partly through the front panel of the instrument.
- Disconnect the EHT cable from the C.R.T. and discharge the cable and the C.R.T.
- Remove the C.R.T. and take care of the C.R.T. socket wiring.
- Remount the new C.R.T. in the reversed sequence.
- If the rubber sleeve around the neck of the C.R.T. must be slid over the neck of a replacement tube, the use of industrial talcum powder is strongly recommended, to prevent the rubber sleeve from sticking on the C.R.T. neck.

9.1.11. Replacing the DELAY LINE UNIT A18

The delay line can be removed after removing the C.R.T. (see section 9.1.10.).

- Remove the C.R.T.
- Disconnect the delay line connections from the vertical amplifier unit (A21) by removing two screws and pulling four miniature plugs.
- The delay line unit itself can be removed by removing the screw of its support bracket which is visible after the C.R.T. is removed.

9.1.12. Removing the rear plate together with the AC POWER UNIT A16

- Remove the six slot headed screws which secure the rear panel.
- Pull out the rear panel.
- Disconnect the three cables and the miniature coaxial plug.
- Unscrew the six screws that secure the unit to the rear panel.

9.1.13. Removing the DC POWER UNIT A15

- Remove the rear panel.
- Remove the internal upper and lower black metal screening plates (2 screws each).
- Disconnect all the seven multipole connectors.
- Unsolder the EHT unit cable and discharge the cable.
- Remove the unit after unscrewing the seven screws that secure the unit to the chassis.

9.1.14. Removing the mains filter

- Remove the rear panel.
- Remove the internal lower black metal screening plate (2 screws).
- Remove the screw that secures the mains filter to the chassis.

9.1.15. Removing the EHT unit A23

- Remove the rear panel.
- Unsolder the EHT unit cable.
- Remove the C.R.T. partly and disconnect and discharge the EHT cable.
- Remove the EHT unit after unscrewing the two ALLEN-screws that fix the unit to the chassis.

9.1.16. Removing the vertical amplifier unit A21

- Remove the three multipole connectors.
- Remove the screening plate from the unit.
- Remove the eight miniature coaxial sockets.
- Remove the delay line connections (see 9.1.11).
- Unsolder the two groups of connections to the trigger unit A22.
- Disconnect the wires which connect the unit to the input sockets A and B and unscrew the screws that secure the unit to these sockets.
- Remove the front panel POWER ON/OFF knob and the plastic axis which is connected to the switch and potentiometer at the rear of the instrument.
- Remove the textplate
- Remove the complete unit after unscrewing twelve screws.

9.1.17. Removing trigger unit A22

- Disconnect all the three multipole connectors from the unit.
- Disconnect the five miniature coaxial plugs from the unit.
- Unsolder the wires that connect the front panel input socket EXT to the unit.
- Unsolder the two groups of connections between this trigger unit and amplifier unit A20.
- Remove the textplate
- The unit can be removed now after unscrewing five screws.

9.2. SOLDERING TECHNIQUES

Working method:

- Carefully unsolder one after the other the soldering tags of the semi-conductor.
- Remove all superfluous soldering material. Use a sucking iron or sucking copper litze wire.
- Check that the tags of the replacement part are clean and pre-tinned on the soldering places.
- Locate the replacement semi-conductor exactly on its place, and solder each tag to the relevant printed conductor on the circuit board.

Note: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the tags must not exceed 250 deg C. The use of a solder with a low melting point is therefore recommended.

Take care not damage the plastic encapsulation of the semi-conductor.

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the oscilloscope.

Suitable soldering irons are:

- ORYX micro-miniature soldering instrument, type 6A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low Voltage Mini Soldering Iron, Type 800/12 W - 6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm-pin-point tip, order no. 4822 395 10012.

Ordinary 60/40 solder and 35- to 40-watt pencil-type soldering iron can be used to accomplish the majority of the soldering. If a higher wattage-rating soldering iron is used on the etched circuit boards, excessive heat can cause the etched circuit wiring to separate from the board base material.

9.3. HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted.
Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed.
Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

9.7. TROUBLE SHOOTING

9.7.1. Introduction

The following information is provided to facilitate trouble shooting. Information contained in other sections of this manual should be used along with the following information to aid in locating the defective component. An understanding of the circuit operation is helpful in locating faults, particularly where integrated circuits are used. See chapter 6 for this information.

9.7.2. Power-up routine

When switching-on the instrument, note that the built-in microprocessor initiates an automatic test of a number of internal circuits including:

- Start test
- PROM test
- LED display test
- RAM test

The sequence and explanation of this power-up routine is as follows:

a) Start test
- Check that about 2 seconds after switching on, pilot lamps REMOTE, RUN, and NOT TRIG'D are ON
- Check that all other pilot lamps and scale lamps are OFF.

This is a visual check only. After this, the next test starts directly.

b) PROM test
This is a check-sum test of all the internal PROM circuits. PROMs 1 to 4 are checked in turn starting with PROM 1.

PROM 1

DISPLAY	SELECT
● ACCU	●
○ STO1	○
○ STO2	○
○ STO3	○

- Check that the ACCU display and select lamps switch ON.

If a fault is found the test sequence stops and no other test is made.
When no fault is found, the next test starts

PROM 2

DISPLAY	SELECT
● ACCU	●
● STO 1	●
○ STO 2	○
○ STO 3	○

- Check that the STO1 display and select lamps also switch ON.

If a fault is found the test sequence stops and no other test is made.
Following a valid test result, the next test starts.

PROM 3

DISPLAY	SELECT
● ACCU	●
● STO 1	●
● STO 2	●
○ STO 3	○

- Check that the STO2 display and select lamps lamps also switch ON.

If a fault is found the test sequence stops and no other test is made.
Following a valid test result, the last PROM test starts.

PROM 4	DISPLAY	SELECT	
	● ACCU	●	– Check that the STO3 display and select lamps also switch ON.
	● STO1	●	
	● STO2	●	
	● STO3	●	If a fault is found the test sequence stops and no other test is made. Following a valid test result, the RAM test will start.

c) LED-display test
Each segment of all the LED-display sections will be switched ON, so that the character will be shown in every section.

All the pilot lamps and scale lamps on the front panel will be switched ON. In this way, the LED-displays and the indicator lamps can be visually checked.
After about 3 seconds the next test is executed.

d) RAM test
This test checks only the micro-processor RAM and not the RAM memories ACCU, STO1, STO2 and STO3.
The RAM part, of which the contents may be destroyed, is now checked by writing and reading a particular pattern.
If a fault is found, the system will stop. If no fault is detected, this RAM part will be cleared.
The RAM part, in which the settings of the channel A and channel B AMPL/DIV switches, the TIME/DIV switch and the trigger delay and their check-sums are stored, may not be destroyed when using the battery back-up facility.
This RAM part will be check-sum tested (in the same way as the PROMS), and cleared when a fault is found (NOP will then be displayed in the alpha-numeric display).

Summary: If the tested circuits are working correctly, all tests will run through in an uninterrupted sequence and after the last test the instrument is ready for use.
In the event of a fault, the test sequence will stop at the point of fault detection.
The test sequence will still continue if a failure occur in one of the pilot lamps or in the alpha-numeric displays.

9.7.3. Trouble shooting aids

Print lay-out and circuit diagrams

The instrument contains a number of functional units. For each of these units a complete detailed circuit diagram and a complete detailed print lay-out drawing is given.

Printed-circuit board lay-out drawings are printed on foldout pages on the left and circuit diagrams are printed on foldout pages on the right, next to each other.
These drawings are located behind the detailed circuit description of the relevant unit.

Electrical values or types of the used components or the component item numbers are shown on the circuit diagram. For the used types of integrated circuits a table is provided.

Each component which is shown on the circuit diagram is marked on the print lay-out drawing by its item number.

Red symbols ▽ on the circuit diagrams are indicating the testpoints which are available on the circuit boards.

Red symbols ○ on the circuit diagrams are indicating all the adjusting elements.

Red symbols □ on the circuit diagrams are giving additional information.

For each integrated circuit and for all the connectors and transformers the pin configuration is given on the circuit diagram.

On the left side of the circuit diagram a part of the print connector is drawn which is giving the connector pin numbers of the incoming signals.
The part of the connector with the outgoing signals and their connector numbers is drawn on the right side of the circuit diagram.

Circuit description

Circuit descriptions (section 6) can be found in the manual in unit number sequence.
Each circuit description gives not only the explanation of the working principle of the unit but also a list of signal denominations and origines and destinations. Furthermore a number of timing diagrams are available.

Locations of adjusting elements

Drawings in section 8 "CHECKING AND ADJUSTING" show the locations of the different adjusting elements to locate these elements rapidly.

I/O addresses

The address codes for the input ports and the output ports are written in the circuit diagrams in hexa-decimal notation. They can be found near to the I/O port circuitries.

9.7.4. Service faultfinding software routines

To facilitate fault finding the PM 3310 is provided with two internal service jumpers. These jumpers can select 3 service routines:

9.7.4.1. Interface test

9.7.4.2. Data-and address-bus test

9.7.4.3. Amplifier and time base setting test

The position of the jumpers, located at the component side of the switch board, is as follows:

Rear view

Note 1: *A service routine can be called only after switching off-and-on the instrument.*

Note 2: *Both jumpers in upper position means normal operation*

Note 3: *Always set the INTENS control fully counter clockwise*

9.7.4.1. Interface test

This test is provided to check the interface functions of microprocessor unit A4. To make this test usefull, the user should know the principles of a microprocessor controlled system and the principles of the PM3310. To start this test, the jumpers at the rear side of the switch board must be set as indicated in the figure at chapter 9-7-4, and afterwards switch-on the instrument again.
The following listing indicates the test sequence, which is executed approximately every 325 μs.

- All alpha-numeric displays are filled with "1"
- To trigger the measuring oscilloscope the SOD pulse at X418 of unit A4 gets active once per cycle
- The pattern AA_H ($1010\ 1010_2$) is written into the output ports: D2424, D2426, D2427 (unit A21); D1326 (unit A13); D414 (unit A4)
  and into the counters D1308 and D1309, D1311 and D1312 (unit A13)
  and into the DAC D1327
- The pattern $3F_H$ ($0011\ 1111_2$) is written into the first address of the ACCU-RAM D601 and D602 (unit A6)
- The TBS pulse is set to 25 kHz by setting $A1_H$ ($1010\ 0001_2$) into output port D1221
- The pattern $3F_H$ ($0011\ 1111_2$) is read out of the ACCU D601 and D602 (unit 6) and written into output port D201.
  This results in lighting of the following scale-and pilot lamps: UNCAL A and B; NOT TRIGD'D RUN and the six scale lamps of the A and B AMPL/DIV switches and the TIME/DIV switch.
- The position of the pushbutton switches DISPLAY are copied to the corresponding SELECT pilot lamps.
- The position of the push-pull-switches INVERT are copied to the corresponding DISPLAY pilot lamps.

NOTE: The ACCU DISPLAY pilot lamp can be tested by the AUTO or DC/AC triggering switches.
DC or AC: ACCU DISPLAY pilot lamp ON.
AUTO : ACCU DISPLAY pilot lamp OFF.

9.7.4.2. Address and data bus test

This test is provided to check the data-and address bus. To start this test the jumpers at the rear side of the switch board must be set as indicated in the figure at chapter 9.7.4., and afterwards switch-on the instument again.
The following listing indicates the test sequence, which is repeated every 3.8 ms.

- All alpha numeric displays shows "2"
- The patterns
  01_H ($0000\ 0001_2$)
  02_H ($0000\ 0010_2$)
  04_H ($0000\ 0100_2$)
  08_H ($0000\ 1000_2$)
  10_H ($0001\ 0000_2$)
  20_H ($0010\ 0000_2$)
  40_H ($0100\ 0000_2$)
  80_H ($10000\ 000_2$)
  are written sequential into the data-ram D601 and D602.
- The above patterns are read out of the data-ram. If the data bus is incorrect the NOT TRIG'D pilot lamp will light. If the data bus is correct the next step is carried out.
- The data Ø Ø H upto and included FFH are written in the data ram on the addresses C Ø Ø Ø H upto and included C Ø FFH.
- The above data are read out of the data ram.
  If the address bus is incorrect the REMOTE pilot lamp will light. If the address bus is correct the test will start again.

9.7.4.3. Front panel switch setting test

This test is provided to copy the settings of the front panel switches (except for the trigger mode and trigger source switches) to the output ports contineously.
Now easy checking of switches, interconnections and output ports is possible.
To start this test, the jumpers at the rear side of the switch board must be set as indicated in the figure of chapter 9.7.4. and afterwards switch-on the instrument again.
The following listing indicates the test sequence:

- All alpha numeric displays are filled with "3"
- The front panel settings are compared and copied into the output ports:

  D2424
  D2426
  D2427
  D1221

- The test repetition time is about 1 ms

9.7.5. Trouble-shooting hints

If a fault appears, the following test sequence can be used to find the defective circuit part:

- Check if the settings of the controls of the oscilloscope are correct. Consult the operating instructions in this manual.
- Check the equipment to which the oscilloscope is connected and the interconnection cables.
- Check if the oscilloscope is well-calibrated. If not refer to section 8 (checking and adjusting).
- Visually check the part of the oscilloscope in which the fault is suspected. In this way, it is possible to find faults such as bad soldering connections, bad interconnection plugs and wires, damaged components or transistors and IC's that are not correctly plugged into their sockets.
- Location of the circuit part in which the fault is suspected: the symptom often indicates this part of the circuit. If the power supply is defective the symptom will appear in several circuit parts.

After having carried out the previous steps, individual components in the suspected circuit parts must be examined:

- Transistors and diodes. Check the voltage between base and emitter (0,7 Volt approx. in conductive state) and the voltage between collector and emitter (0.2 Volt approx. in saturation) with a voltmeter or oscilloscope. When removed from the p.c.b. it is possible to test the transistor with an ohmmeter since the base/emitter and base/collector junctions can be regarded as diodes. Like a normal diode, the resistance is very high in one direction and low in the other direction. When measuring take care that the current from the ohmmeter does not damage the component under test.
  Replace the suspected component by a new one if you are sure that the circuit is not in such a condition that the new one will be damaged.
- Integrated circuits. In circuit testing can be done with an oscilloscope or voltmeter. A good knowledge of the circuit part under test is essential. Therefore first read the circuit description in section 6.
- Capacitors. Leakage can be traced with an ohmmeter adjusted to the highest resistance range. When testing take care of polarity and maximum allowed voltage. An open capacitor can be checked if the response for AC signals is observed. Also a capacitance meter can be used: compare the measured value with value and tolerance indicated in the parts list.
- Resistors. Can be checked with an ohmmeter after having unsoldered one side of the resistor from the p.c.b. Compare the measured value with value and tolerance indicated in the parts list.
- Coils and transformers. An ohmmeter can be used for tracing an open circuit. Shorted or partially shorted windings can be found by checking the wave-form response when HF signals are passed through the circuit. Also an inductance meter can be used.
- Data latches. To measure on inputs and outputs of data latches a measuring oscilloscope can be triggered by the clock signal which is connected to the clock input of the data latch.
  Check the input data lines one by one during the active edge of the clock signal.
  This measurement can only be done in this way when there is an acceptable repetition time of the clock signal. A too low clockpulse repetition time results in a low intensity of the trace on the C.R.T. screen of the measuring oscilloscope.
  The outputs can easily be checked for correct data by an oscilloscope or voltmeter

Oscilloscope checking of micro-processor bus signals

The 8085 micro-processor (D408) is provided with the following busses:
- Address bus
- Data bus
- Control bus

In general, if signals on these bus lines are checked with an oscilloscope, a very unstable display will be the result.
This is due to the fact that these signals vary with time in a rather unpredictable way.
If anyhow a stable display of signals from one of these busses is obtained, this may be an indication that the micro-processor runs in a small program loop.

Note: *Note:*

If a component must be replaced always use a direct-replacement. If not available use an equivalent after carefully checking that it does not degrade the instrument's performance. See also section 9.1. (replacement).
After replacement of a component the calibration of the instrument may be affected due to component tolerances. If necessary do the required adjustments.

Most of the test measurements can be carried out with a 2-channel oscilloscope and a voltmeter.
Use of a 4-channel oscilloscope with delayed time-base (e.g. PM 3244 or PM 3264) is recommended.
A number of measurements can also be done with a correct triggered logic analyzer.
Probes must be earthed near to the measuring points.

9.7.6. Overall view of provisions and service methods especially for fault location in various digital circuitries of the instrument.

FRONT BOARD A201

The data to be displayed in the alphanumeric displays and the pilot lamps can be measured in the following way:

Pilot lamps

Trigger an oscilloscope with the clock signal on point 11 of the relevant latch D201 or D202 and check the data lines D0 ... D7 one by one during the positive going edge of the clock signal.
The data outputs can easily be checked for correct data by an oscilloscope or voltmeter.

Alphanumeric displays

Trigger the main time-base of an oscilloscope externally with the "DELAY LOOP TRIGGER" which is available on test point X412 of unit A4.
Connect the signal $\overline{IOA}$ on point C21 of connector X424 on unit A4, with channel A of the oscilloscope and set the TIME/DIV switch to 0.2 ms/div.
A group of 16 negative going $\overline{IOA}$ pulses is displayed now.
Select this group of 16 pulses with the aid of the delayed time-base in such a way that a triggered display of 16 pulses divided over the whole ten divisions of the screen is obtained.
The first $\overline{IOA}$ pulse belongs to address 80A0H and the last $\overline{IOA}$ pulse belongs to address 80AFH.
By connecting the data lines D0 ... D7 one by one to the B channel of the oscilloscope the data can be checked.

Set the oscilloscope for this check in ALT-mode and use the TBMAGN and XPOSITION controls.

SWITCH BOARD A202

For measuring on the switch board the instrument has to be set in the SERVICE ROUTINE NUMBER 3 (page 9-16) with the jumpers on unit A202.

Switches

The output signals of the front panel switches can be measured with a normal voltmeter on the CIS connectors or the input of the multiplexer's D241-D242-D243-D247-D248 and D249.
Signals can be checked while operating the relevant switches.

Multiplexers

Trigger the MAIN TIME-BASE of a dual channel oscilloscope with one of the signals $\overline{RDF0}$ - $\overline{RDF2}$ or $\overline{RDF4}$ connected to the channel A input.
RDF0 is available on testpoint X246 on unit A202
RDF2 is available on testpoint X244 on unit A202
RDF4 is available on testpoint X243 on unit A202
Set the measuring oscilloscope in 5 μs/div. - DC - TRIG - SLOPE "—" and correct LEVEL.

Connect the data lines D0 ... D7 one by one to the channel B input and check the data during the positive going edges of the trigger signal on channel A when operating the relevant front panel switches.

MICROPROCESSOR UNIT A4

Every $\approx$ 20 ms a number of trigger pulses are generated by the software for test purposes.
- Trigger pulse "START MAINLOOP" is available at X407.
- Trigger pulse "START DISPLAY LOOP" is available at X409.
- Trigger pulse "START DELAY LOOP" is available at X412.

Latches and bidirectional buffer D413 - D414 - D416 and D417 are placed in sockets and can be easily removed from the unit for test purposes.
- Removing D413 results in disconnecting the internal address bus from the internal address/data bus.
- Removing D414 results in disconnecting the output port from the system.

– Removing D416 results in disconnecting the system address bus from the internal address/data bus.
– Removing D417 results in disconnecting the system data bus from the internal address/data bus.

This can for example be used to separate and locate the fault in case of a short-circuit in one of the busses.

The unit contains a number of soldering spots with the following functions:
– Signal RST 7.5 can be connected to the +5 V for test purposes.
  This is not of interest for servicing in standard instruments.
– PROM address line A11* can be disconnected from the +5 V and connected to address line A11 from the microprocessor.
  This is necessary in case the IEC option PM 3325 is used because of the use of a PROM circuit D407 of 4096 x 8 bits.
– For test purposes the $\overline{\text{RESIN}}$ input circuit (watchdog circuit) can be replaced by a simple reset circuit with C411.
– The TRAP input circuitry can be made inactive for service purposes.

To measure the signals ZEN - INV and CLDT, the measuring oscilloscope must be triggered with the signal on X407 (START MAINLOOP).

– ZEN can be checked by operating the front panel display select switches.
– INV can be checked by operating the front panel invert switches for STO1-2 and 3.

The input data lines for the latch D414 can be measured with the method described in section 9.7.5.

Fault finding method

– Check supply voltages.
– Check whether the "START MAIN LOOP" trigger is present once every 20 msec at testpoint X407 on unit A4 or not.
– Check if the μP is switched in the HOLD-state. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are then switched to about 1.5 V (can be done via input TRAP for example).

– Disconnect TRAP input (solder spot).
– Disconnect the WATCHDOG circuit and connect C411 to $\overline{\text{RESIN}}$ (solder spot).
– Replace eventually the μP itself.
– Replace eventually the PROM circuits.
– Check the busses for short circuits or interrupts. For this, latches and bidirectional buffers can be removed from their sockets.

After the repair everything must be brought in the normal position again.

RAM UNIT A6

Tri-state buffer D617 can be removed from its socket so that no data can be placed on the system data bus by the RAM unit.

BUFFER UNIT A7

A solder spot is available in the CLKSH circuitry for test purposes. So a CLKSH can be derived from signal C4 which is generated during the time that the ADC output is placed on the ADC bus. The ADC output contents can then directly be placed in the shift register without correction.

Using this facility in combination with the interruption of signal line DAC M-1, results in the switching off of the total correction circuitry.

After the repair everything must be brought in the normal position again.

For test purposes in ROLL-mode, the ROLL-mode action can be done 5000 times faster by placing jumper S1201 in the left position.

Check for correct time-base setting

Select service test routine number 3.
The TIME/DIV switch position is now read by the microprocessor and this processor in turn will set the belonging code (according to the table on page 6-136) on the data lines D0 ... D7 so that it can be latched by latch D1221 on unit A12.

These codes can be measured on the inputs of latch D1221 by triggering a monitor oscilloscope with the clock signal on D1221-pt. 11. Now the data lines can be observed one by one during the active edge of the clock signal. Codes on the outputs of the latch can be measured with a voltmeter or an oscilloscope.

In this way the correct functioning of the TIME/DIV switch, the microprocessor and the latch D1221 can be checked for RECURR-mode as well as for ROLL-mode. (In ROLL-mode D5 will steady be "0") and different TIME/DIV switch positions.
Now all the dividers and multiplexers can be checked for all the TIME/DIV switch positions in a simple way.

ROLL-mode check 0.5 s/div ... 60 min/div

- Depress pushbutton ROLL.
- Set jumper S1201 in the left position.
- Measure the TBS signal on D1219 - point 7 with an oscilloscope and check the signal repetition time in accordance with the table below.

TIME/DIV switch setting	Signal repetition time
60 min/div	28,80 ms
30 min/div	14,40 ms
15 min/div	7.20 ms
6 min/div	2.88 ms
2 min/div	0.96 ms
1 min/div	0.48 ms
0.5 min/div	0.24 ms
20 s/div	160 µs
10 s/div	80 µs
5 s/div	40 µs
2 s/div	16 µs
1 s/div	8 µs
0.5 s/div	4 µs

- Set the jumper S1201 again in the right position.

RECURR-mode check 0.2 s/div ... 0.5 ms/div

- Depress pushbutton RECURR.
- Measure the TBS signal on D1219 - point 7 with an oscilloscope and check the signal repetition time in accordance with the table below.

TIME/DIV switch setting	Signal repetition time
0.2 s/div	8 ms
0.1 s/div	4 ms
50 ms/div	2 ms
20 ms/div	800 µs
10 ms/div	400 µs
5 ms/div	200 µs
2 ms/div	80 µs
1 ms/div	40 µs
0.5 ms/div	20 µs

RECURR-mode check 0.2 ms/div ... 0.5 µs/div

- Depress pushbutton RECURR.
- Measure the TBF signal on X1206 in accordance with the table below.

TIME/DIV switch position	Signal repetition time
0.2 ms/div	8 µs
0.1 ms/div	4 µs
50 µs/div	2 µs
20 µs/div	0.8 µs
10 µs/div	0.4 µs
5 µs/div	0.2 µs
2 µs/div	0.08 µs
1 µs/div	0.04 µs
0.5 µs/div	0.02 µs

DELAY TRIGGER UNIT A13

There are two solder spots available on the unit. One to invert the PENLIFT output signal and a solder spot to connect the input trigger TRIST directly with the output signal line DELTRG.
In this way the whole delayed trigger circuit is switched off, and the trigger point is at the right-hand side of the CRT screen.

Check for correct latch, delay counter and DAC delay setting

The input data lines for the latch D1326, the counters D1308 - D1309 - D1311 and D1312 and the DAC DELAY D1327 can be measured with the method described in section 9.7.5.

Trigger signals

D1324 - pt. 8	for data latch D1326
D1324 - pt. 6	for MSB of delay counter
D1324 - pt. 12	for LSB of delay counter and for DAC DELAY

The delay counter (used in D- and P-mode) is set according to the formula:

$$\text{Counter setting} = \{(10+N) * 5+8\}$$

In this formula N is the number of divisions set by the user ($-9 \leqslant N \leqslant 9999$).
Note that the four least significant bits the inverted information is placed on the data bus.

The DAC DELAY (used in S-mode) is set in the following way:

$$\text{DAC DELAY setting} = 2 * N$$

N is the number of divisions set by the user ($0 \leqslant N \leqslant 100$)

DC POWER SUPPLY A15

Dummy load for PM 3310 power supply

Voltage	Load resistance	
– 12 V	15.6 Ω	(3 x 47 Ω //)
+ 12 V	15.6 Ω	(3 x 47 Ω //)
– 6 V	40 Ω	(47 Ω // 220 Ω)
+ 6 V	40 Ω	(47 Ω // 220 Ω)
– 5.2 V	5 Ω	(2 x 10 Ω //)
+ 5 V	2.5 Ω	(4 x 10 Ω //)
+ 40 V	300 Ω	
–125 V	10 kΩ	
+125 V	10 kΩ	

INPUT AMPLIFIER UNIT A21

Check for correct latch setting

The input data lines for the latches D2424 - D2426 and D2427 can be measured with the method described in section 9.7.5.

Multiplexer check

Trigger the MAIN-TIME-BASE of a dual channel oscilloscope with the external trigger signal "MAIN LOOP TRIGGER" which is available on testpoint X407 on unit A4.
Connect the signal on point 6 of D2423 on unit 21 with the channel A of the oscilloscope and set the TIME/DIV switch to 20 µs/div.
Two negative going pulses are displayed now.
Select these two pulses with the aid of the delayed time-base in such a way that a triggered display of these two pulses is obtained.
During the first pulse multiplexers D2418 and D2419 are set to the "T" position and during the second pulse they are set to the "1" position.
By connecting the data lines D0 ... D7 one by one to the B channel of the oscilloscope the data can be checked.

Checking the protective leads

The correct connection and condition is checked by visual control and by measuring the resistance between the protective-lead connection at the plug and the cabinet.
The resistance should be $< 0{,}5\ \Omega$. During measurement the mains cable should be moved. Resistance variations indicate a defect.

Checking the insulating resistance.

Measure the insulating resistance at $U_{dc} = 500$ V between the mains connections and the protective lead connections.
For this purpose set the mains switch to ON. The insulating resistance should be $> 2\ M\Omega$.

10. INTRODUCTION TO MICROPROCESSORS

10.1. A BRIEF ENCOUNTER

Microcomputers, like people, do not reveal all their secrets at a brief encounter. If this is your first introduction to a microcomputer, you will need a little time to familiarise yourself with its characteristics — what it can do, how it does it and how its facilities are best used to advantage.

As its name implies, a microcomputer is an extremely small device.
Extremely small because it is based on a silicon-chip microprocessor.

The great future predicted for the microprocessor lies in its *enormous work capacity* for processing signals, available within *negligible physical capacity*.

The human brain has the ability to determine by calculation in a more sophisticated way, but our microcomputer, with its built-in 'one-track' mind, is capable of much faster calculation speeds. Also the computer facilities extend beyond the confines of the brain and memory to perform some of the functions we allocate to other parts — the eyes, ears, arms and legs.

Besides the ability to store and manipulate information, the microprocessor circuits are capable of recognising visual, aural and physical conditions, evaluating them and presenting them in a form required by an instrument or operator. A practical application of this could be the monitoring of strain-gauges or thermometers in an industrial process at regular intervals and the recording of the values, together with any alarm conditions, on a print-out. In contrast to this data logging function, the microcomputer could be an integral part of a laboratory measuring instrument; e.g. a digital oscilloscope, for control, storage and read-out purposes.
Microcomputers are designed with built-in flexibility to enable them to be used for a wide variety of applications. This versatility is obtained in the signal conditioning circuits that present the data to the computer central processing unit in a form that it can readily understand. In electronics, the simplest and most reliably defined condition is when a circuit is either switched on or switched off. This two-state notation of defining the numerical terms of a problem is universally used in computers and is known as the binary system.

10.2. COMING TO TERMS

After a general picture of the microcomputer field, it is useful to look a little closer at the practical aspects and to discuss some of the terms that are in everyday use.

Microcomputer	A miniature electronic system that performs arithmetic and logic operations on data according to a programmed sequence of instructions stored in a memory. As a calculating system, the microcomputer consists not only of the physical components (the hardware) but also of program instructions (the software).
Hardware	The mechanical, electronic and electromechanical components of the computer system.
Software	The programmer's language for communicating with the computer. This includes sets of programs translated into binary form to enable the computer to perform specific functions as required by the system user.

Microprocessor CPU

The heart of the microcomputer, the central processing unit (CPU) that performs all the functions as arithmetic and logic operations that are written in the system software program. In addition to the Arithmetic and Logic Unit (ALU) it also contains a Control Block and Register Array.

Memory

A high-speed electronic device in which data and instructions are stored for subsequent processing.

Input/Output

Devices that provide communication between the microcomputer system and the outside world. For example, interfacing input data and instructions via a keyboard and outputting results via a display unit or printer.

Instruction set

A set of characters that define an operation with generally one or more addresses, which are given via the input device and can be stored in the memory. When a program is running, data-words are processed in a sequence and manner as specified by the instructions, the results being stored and/or outputted via an output device.

Data word

A word, or group of binary digits (bits) used to encode data, as distinct from an instruction word. A byte is a word of 8 bits.

Binary notation

A system of numbering used in computers that uses 2 as a base in contrast with the normally used decimal system that has 10 as a base. Only two symbols are required in the binary system, 0 and 1, which can be conveniently represented in electronic circuits as two voltage levels in a signal. The binary equivalents of the decimal numbers 0 to 10 are as follows:

DECIMAL		BINARY
0	=	0000
1	=	0001
2	=	0010
3	=	0011
4	=	0100
5	=	0101
6	=	0110
7	=	0111
8	=	1000
9	=	1001
10	=	1010

Addition:

DECIMAL	BINARY
5	0101
+9	+1001
14	1110

To add binary numbers, proceed as in decimal but remember that the radix is 2. i.e. carry 1 when 2 is reached.

Hexadecimal notation

Using 16 as a base this system provides a short-band method of writing 4-bit binary numbers with alphanumeric symbols. This is useful for a data-word grouped as a 4-bit field, where there are 16 combinations.

COMBINATION	BINARY CODE	HEXADECIMAL CODE
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
10	1010	A
11	1011	B
12	1100	C
13	1101	D
14	1110	E
15	1111	F

Analog-to-Digital Converter

Enables physical or electrical input signals that are in analog form to be converted to digital form for processing in the computer.

Register

Consists of a group of two-state flip-flops, which by means of a clock-pulse command can store the data-word present on its input lines.
The output lines remain stable until a new data-word is clocked into the register. A group of registers forms a memory.

Data-bus

Enables several circuits to communicate with each other without the need for separate data paths. This databus is common to all circuits and a timing and control circuit organises which circuits use the databus at any particular time, in conjunction with an ADDRESS-BUS and a CONTROL-BUS.

Address-bus

Enables memory locations to be addressed by their unique device numbers.

Control-bus

Controls the exact timing of the communication on the data-bus and also the direction of data flow.

10.3. SYSTEM FEATURES

With a basic understanding of the language and hardware component parts of a microcomputer it is interesting to discover how these can be integrated to form an organised system. The following illustrations show the basic system features which, for greater comprehension, should be studied with reference to the computer terms that have been previously defined.

Basic features

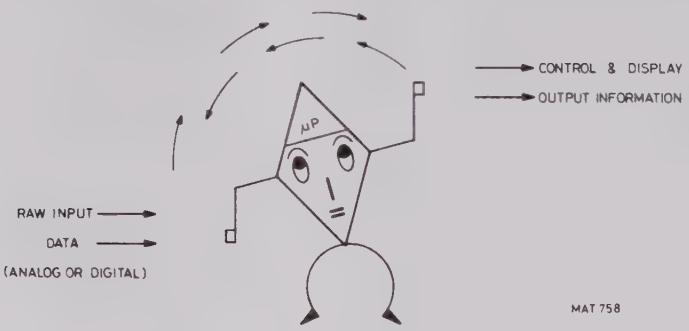


Fig. 10.3.1.

In simple terms, our Master Microcomputer takes data with one hand, juggles with it, and hands it out with the other. Being highly intelligent, its right hand definitely knows what its left hand is doing!

Input features

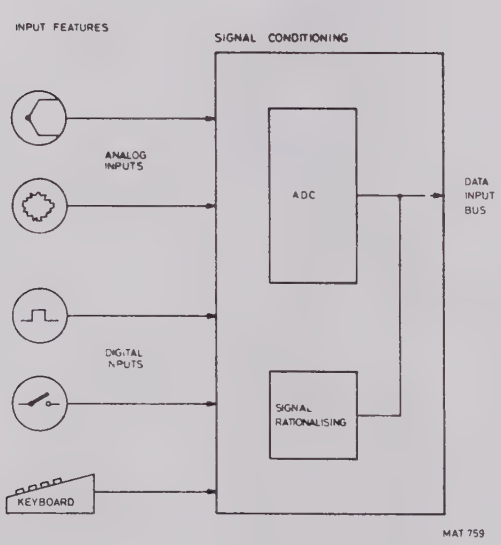


Fig. 10.3.2.

The raw inputs from analog sources such as thermocouples, strain-gauges voltage and current devices, etc., must first be converted to the digital form required by an ADC in the signal conditioning part of the microcomputer.
Digital inputs from switch contacts, logic levels from sold-state devices or from counters, etc., must be converted to the correct logic levels within the signal conditioning part.

Output features

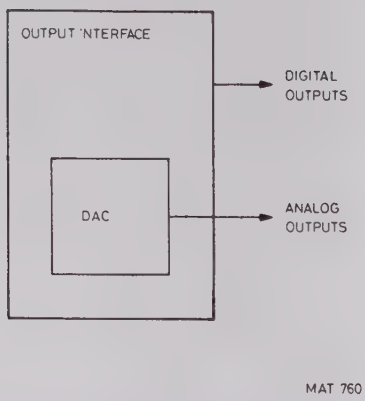


Fig. 10.3.3.

The output interface circuits are designed to present the output data in a form suitable for the various system requirements, e.g. digital displays, print-outs, parallel and serial interfaces, alarms, etc. When analog output signals are required, digital-to-analog conversion (DAC) is performed in the computer output interface circuits.

Memory features

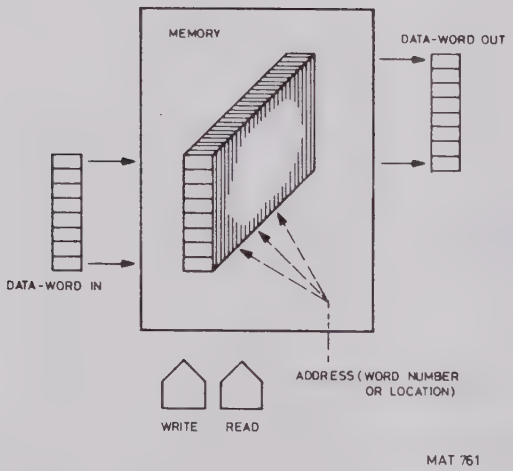


Fig. 10.3.4.

A memory is simply a group of registers used for storing data-words, for future retrieval when required. With a WRITE pulse, a data-word can be stored; a READ pulse enables a data-word to be read out of a location.
An ADDRESS must be provided with the READ and WRITE pulses to locate the specified data-word.
Memories can be used for storing signal data or for programming instructions. Instruction sets for microcomputers are usually stored in read-only memories, ROMs or PROMs (Program Read Only Memories).

The memory contains not only the information to tell the microprocessor what to do, but also the instructions on how to do it.
Variable data are usually stored in random-access memories, RAMs.

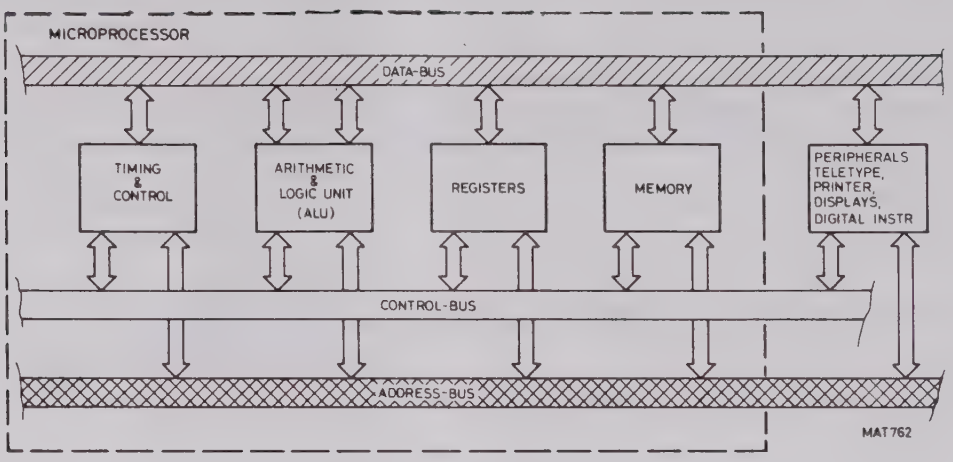


Fig. 10.3.5.

The elementary circuits of a microcomputer comprise:
- registers
- a memory (ROM + RAM)
- a data-bus, control-bus and address-bus
- a data-bus, timer and controller circuit
- an arithmetic and logic unit (ALU)

If the integrated circuit contains no memory, or only a limited memory, we refer to this as a microprocessor. The microcomputer, together with its memory and the peripheral equipment constitute the hardware of the system.

Programming features

In order to perform meaningful operations with the hardware of a computer system, we need to specify precisely:
- what OPERATIONS are required upon a defined DATA-WORD
- in what SEQUENCE these will occur
- to which LOCATION the results of the operation have to be deposited.

This process of prescribing the necessary actions within a computer system is called PROGRAMMING the computer software.
Programming consists of the sequential execution of the instructions stored in the memory, under the control of the TIMING and CONTROL part. Its circuits decode the instruction and initiate the necessary data-word transports and operations.
A basic flow-chart cycle for each instruction is as follows:

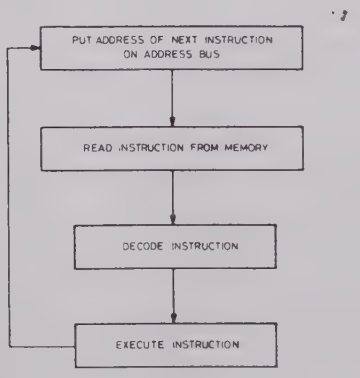


Fig. 10.3.6.

A PROGRAM COUNTER is a special register equipped to increment the address of sequential instructions to enable new instructions to be FETCHED from the memory. As the program counter is connected to the data-bus, the contents can be replaced by other values to permit a JUMP to an instruction elsewhere in the memory.

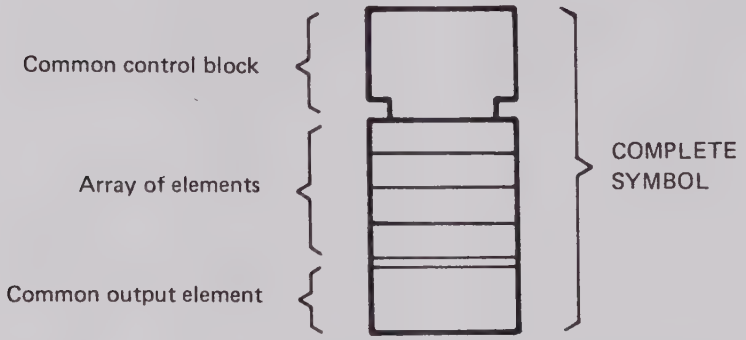
As the execution of an instruction consists of a number of sub-steps, it is useful to be able to store an instruction temporarily in a register if the next operation needs to use this result. The two operations are combined in a single register, called the ACCUMULATOR for ease of presentation to the ALU in the next instruction.
Apart from the memory, microcomputers usually have some general-purpose registers to store intermediate results on a temporary basis.

Note: For more information refer to:
"INTRODUCTION TO MICROPROCESSORS AND THEIR USE IN T&M INSTRUMENTS".
Ordering number: 9499 990 00711.

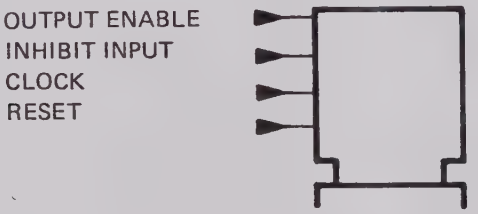
11. EXPLANATION OF USED SYMBOLS

I NTRODUCTION

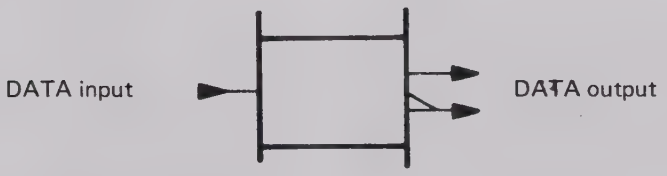
Common control block
The use of binary logic integrated circuits (M.S.I.'s) necessitated an abbreviated notation for the interdependency of various functions, as well as simplified symbols for complex functions.
The most important information is: which signals appear at the input and how the outputs behave with respect to the function of the IC.



Common control block
On the common control block, all **common** input lines are connected. These lines must have funtional relation to the other elements of the symbol. Examples: general reset, output enable, inhibit input, clock signal etc.

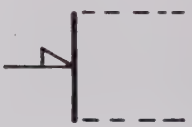
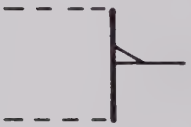
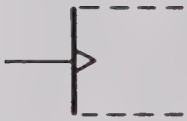
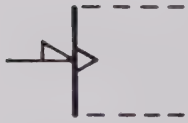
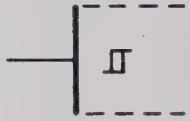
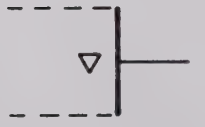
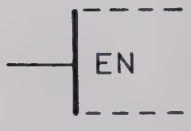


Array of elements
Each element of the array has its own in-and outputs. Example: it can be a D-flip-flop with one data input and two outputs (one inverted and the other not inverted).

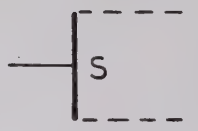


LIST OF CHARACTERS AND SYMBOLS

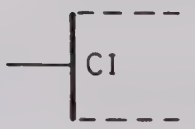
In the common control blocks, characters and symbols are used to indicate the function of the in-and outputs.

SYMBOL	DESCRIPTION
	Polarity indicator at input
	Polarity indicator at output
	Dynamic input
	Dynamic input with polarity indicator
	Schmitt - trigger input
	Open collector output
	Tri-state output
	D - input
	Enable input

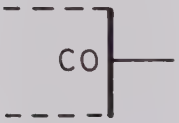
Forcing reset input



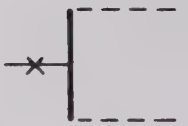
Forcing set input



Carry input of an arithmetical element

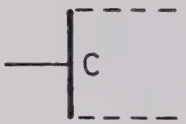


Carry output of an arithmetical element

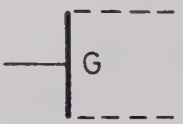


Line carrying no logic information (input)

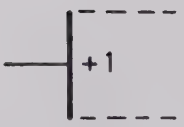
Line carrying no logic information (output)



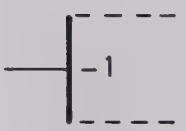
Clock input



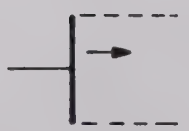
G — input implying an AND— relationship



Count up command for counters



Count down command for counters



Shift right (down) command for shift register

Shift left (up) command for shift register

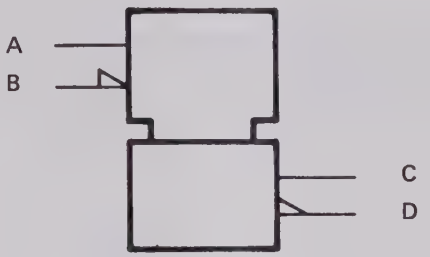
Common output element

On the common output element the common or resulting outputs of the elements are drawn.

Example: it can be a carry or a borrow signal for a counter.

Input and output lines

Input lines are drawn at the left side of a symbol, output lines at the right side. In-and output lines can be drawn with and without ◺ as shown.



Meaning of the above-drawn lines A, B, C and D:

- Line A is active for the block when it is high ("1") and inactive when it is low ("0") .
- Line B is active for the block when it is low ("0") and inactive when it is high ("1").
- Line C is low ("0") in the rest state of the element or when output is inhibited. This output is then inactive.
- Line D is high ("1") in the rest state of the element or when output is inhibited. This output is then inactive.
- When line C is "high", this output is active.
- When line D is "low", this output is active.

DEPENDENCY NOTATION

1. Introduction

Dependency notation is a means of denoting the relationship between inputs, outputs and between inputs and outputs, without actually showing all the element and interconnections involved.

Apart from its use in complex element, dependency notation should not be used to replace the symbols for combinative elements.

The information provided by dependency notation **supplements** that provided by the qualifying symbol for an element's function.

In the convention for the dependency notation, use is made of the terms "affecting" and "affected". In the case where it is not evident which inputs must be considered as being the affecting or the effected ones (e.g. if they stand in an AND-relation), the choice may be made in any convenient way.

Ten different kinds of dependency have been defined.
They are:

A	ADDRESS	– dependency
C	CONTROL	– dependency
EN	ENABLE	– dependency
G	AND	– dependency
M	MODE	– dependency
N	NEGATE	– dependency
R	RESET	– dependency
S	SET	– dependency
V	OR	– dependency
Z	INTERCONNECTION	– dependency

Each dependency is represented by a capital letter or letter combination, as shown above.

AND–, OR– and NEGATE–dependencies are used to denote Boolean relationships between inputs and/or outputs. INTERCONNECTION-dependency is used to indicate that an input or output is connected to one or more inputs and/or outputs.

CONTROL–dependency is used to identify a timing-input or a clock-input of a sequential element and to indicate which inputs are controlled by it.
SET– and RESET–dependencies are used to specify the internal logic states of an RS bistable element in the case that the R– and S–inputs both stand at their internal 1–states.
ENABLE–dependency is used to identify an ENABLE–input and to indicate which inputs and/or outputs are controlled by it (e.g. which outputs take on their high impedance state).
MODE–dependency is used to identify an input which selects the mode of operation of an element and to indicate the inputs and or outputs depending on that mode.
ADDRESS–dependency is used to identify the ADDRESS inputs of a memory.

The table below lists the various dependencies and summarizes their effects. In this table the word "action" implies:

– that affected inputs will have their normally defined effect on the function of the element;

– that affected outputs will take on the internal logic states as determined by the function of the element.

2. Convention

a. Dependency notation usually defines relationships between internal logic states. However in the case of 3–state outputs and open circuit outputs, ENABLE–dependency defines relationship between the internal logic states of affecting inputs and the external states of affected outputs.

b. Application of dependency notation is accomplished by:
- labelling the affecting input or output with the relevant letter followed by an identifying number;
- labelling each input or output affected by that affecting input or output with that same number;
- labelling each input or output affected by the **negated** internal logic state of the affecting input or output with that same number with a bar over it.

c. If the affected input or output already has a label, denoting its function, this label must be prefixed by the identifying number of the affecting input.

d. If an input is affected by more than one affecting input or output, the identifying number of each of the affecting inputs or outputs shall appear in the label of the affected one, separated by commas. The normal reading order of these identifying numbers is the same as the sequence of the affecting ralationship.

e. Two affecting inputs labelled with different letters, must not have the same identifying number, unless when one of the letters is A.

f. If two affecting inputs or outputs have the same letter and the same identifying number, they stand in an OR–relation to each other.

g. If an affected input or output already has a label which would form an ambiguous combination with the identifying number, the latter must then be replaced by a different character (e.g. Greek letter) to avoid ambiguity.

h. An affecting input or output affects only the corresponding affected input or outputs of the element.

Type of dependency	Letter(s)	Effect on affected input or output if the affecting input stands at its internal 1–state	0–state
ADDRESS	A	permits action (address selected)	prevents action (address not selected)
CONTROL	C	permits action	prevents action
ENABLE	EN	permits action	– prevents action of affected inputs – imposes external high-impedance state on open-circuit and 3-state outputs (internal state of 3-state outputs unaffected) – imposes 0-state on other outputs
AND	G	permits action	imposes 0-state
MODE	M	permits action (mode selected)	prevents action (mode not selected)
NEGATE	N	complements state	no effect
RESET	R	affected output reacts as it would to S=0, R=1	no effect
SET	S	affected output reacts as it would to S=1, R=0	no effect
OR	V	imposes 1-state	permits action
INTERCONNECTION	Z	imposes 1-state	imposes 0-state

12. PARTS LISTS

(subject to alteration without notice)

The opening of parts, or removal of covers, is likely to expose live conductors. The instruments should therefore be disconnected from all voltage sources before any opening of parts or removal of covers is started.
During and after dismantling, bear in mind that capacitors in the instrument may still be charged even if the instrument has been separated from all voltage sources.
Item numbers (e.g. C R V) have been divided in groups which relate to the circuit, the unit and the circuit diagram, according to the following table.

Item numbers	Location	Unit number
100 . . . 199	Front side unit	A1
200 . . . 299	Front unit	A2
300 . . . 399	Mother board unit	A3
400 . . . 499	Microprocessor unit	A4
500 . . . 599	Spare unit	A5
600 . . . 699	Ram unit	A6
700 . . . 799	Buffer unit	A7
800 . . . 899	Conversion unit	A8
900 . . . 999	ACL unit	A9
1000 . . . 1099	CCD logic unit	A10
1100 . . . 1199	P^2CCD unit	A11
1200 . . . 1299	Time-base unit	A12
1300 . . . 1399	Delay trigger unit	A13
1400 . . . 1499	IEC unit (OPTIONAL)	A14
1500 . . . 1599	DC POWER UNIT	A15
1600 . . . 1699	AC POWER UNIT	A16
1700 . . . 1799	Rear side unit	A17
1800 . . . 1899	Delay line	A18
1900 . . . 1999	CRT socket	A19
2000 . . . 2399	Final ampl. unit	A20
2400 . . . 2699	Ampl. unit	A21
3000 . . . 3099	Ampl. unit	A21
2700 . . . 2999	Trigger unit	A22
3100 . . . 3199	EHT unit	A23

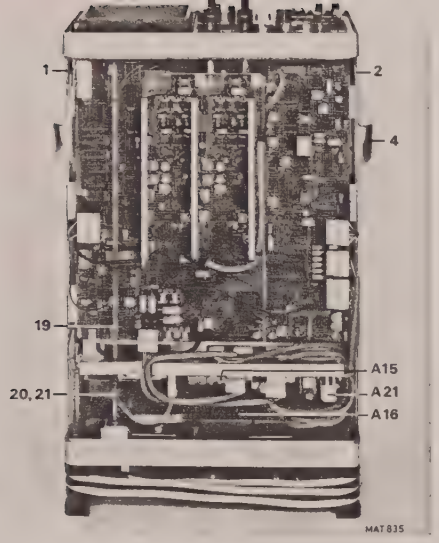


Fig. 12.1.1.

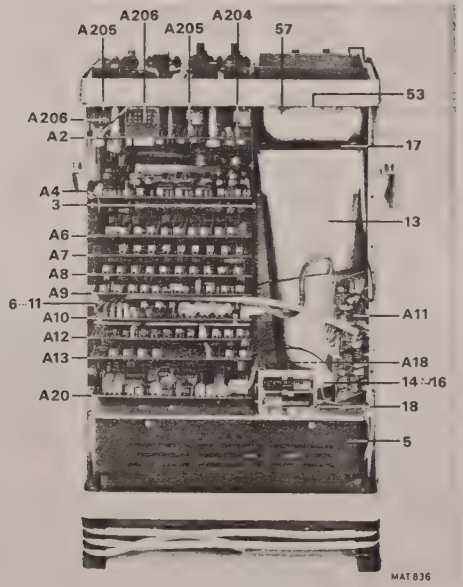


Fig. 12.1.2.

12.1. MECHANICAL PARTS

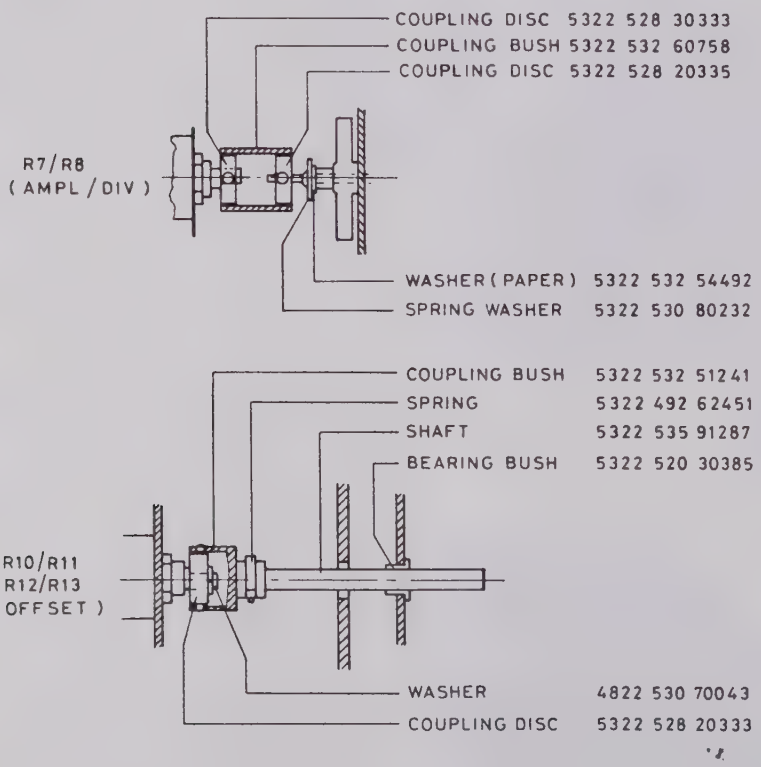
Item	Qty	Order number	Description	
1	1	5322 460 64042	Side profile left	
2	1	5322 447 94625	Side profile right	
3	2	5322 462 34199	Print support	
4	2	5322 528 34113	Arret for handle	
5	2	5322 447 94638	Cover top and bottom	
6	1	5322 815 22804	Cil bolt M4X6	
7	1	4822 505 10488	Square nut M4	
8	1	5322 532 14593	Washer 4. 3X12	
9	1	4822 530 80077	Spring washer 5,2	
10	1	5322 815 28054	Cil bolt M3X8	
11	1	4822 532 10332	Washer 3. 2X7	
12	1	4822 530 80173	Spring washer	
13	1	5322 462 54154	CRT shielding	
14	1	5322 492 64767	Clamping strip	
15	1	4822 502 10051	Cil bolt M4X20	
16	1	4822 505 10488	Square nut M4	
17	1	5322 466 64213	Plastic profile 30cm	
18	1	5322 256 64014	Battery holder	
19	1	5322 535 94978	Shaft assy	
20	1	5322 532 24398	Coupling	
21	2	4822 502 10668	Screw for coupling	
22	1	5322 455 84091	Textplate	
23	3	5322 414 34134	Knob dia 10	
24	3	5322 492 64337	Clamping spring knob	
25	9	5322 414 34091	Knob dia 10 shaft 6	
26	2	5322 414 34249	Attenuator knob assy	
27	1	5322 414 34261	Time/div knob assy	
28	3	5322 532 54478	Distance washer	
29	2	5322 462 44458	Housing	Range indication instrument parts.
30	2	5322 462 44459	Cover	
31	2	5322 492 54338	Compression spring	
32	2	5322 268 14157	Contact pin	
33	1	5322 466 85887	Cover for IEC conn.	
	1	5322 480 34074	Contrast filter acc.	
37	1	5322 466 74059	Bezel	
38	1	5322 480 34046	Contrast filter	
39	1	5322 447 94169	Front cover	
40	1	5322 447 94626	Top cover	
41	1	5322 466 64214	Adhesive strip	
42	1	5322 447 94627	Bottom cover	
43	1	5322 455 84092	Text strip	
44	1	5322 498 54042	Aluminium profile	
45	1	5322 498 54045	Plastic profile	
46	2	5322 535 74401	Locking pin	
47	2	5322 492 54155	Compression spring	
48	1	5322 498 54044	Bracket left	
49	1	5322 498 54043	Bracket right	
50	5	5322 414 74029	Knob cover blue + line	
51	7	5322 414 74015	Knob cover grey + line	
52	1	5322 414 74019	Knob cover grey	
53	2	5322 380 24089	Light reflector assy	
54	1	5322 290 64085	Soldering support	
55	1	5322 255 44088	Led holder	
56	1	5322 505 14184	Nut for cal terminal	

Item	Qty	Order number	Description	
57	2	5322 255 24015	Lamp holder	
58	4	5322 535 84447	Extension part (01 version)	
58	4	5322 462 50215	Extension part (02 and up)	S29
59	4	5322 414 25613	Push button + green (01 version)	
59	4	5322 414 26415	Push button + green (02 and up)	
60	1	5322 505 14178	Knurled nut	
61	1	5322 466 85888	Locking plate	
62	1	5322 532 24579	Bush	
63	1	5322 532 14697	Washer	
64	1	5322 290 34022	Soldering tag	
65	1	5322 506 14001	Nut	
66	2	5322 505 14186	Nut	
67	2	5322 532 34124	Spacer	
68	2	5322 532 24374	Coupling R7-R8	
69	8	5322 414 14011	Push button grey (01 version)	
69	8	5322 414 25851	Push button grey (02 and up)	
70	2	5322 414 26019	Push button L. grey (01 version)	
70	2	5322 414 20002	Push button L. grey (02 and up)	
71	35	5322 535 84447	Extension part switch (01 version)	
71	35	5322 462 50215	Extension part switch (02 and up)	
72	6	5322 532 54492	Paper washer 2.2X5	
73	2	5322 278 74008	Arret for switch	
74	2	5322 535 94966	Inner shaft	
75	1	5322 278 74009	Arret for switch	
76	6	5322 255 34122	Lamp holder	
77	10	5322 532 60487	Ceramic spacer	
78	6	5322 255 44218	IC-FOOT 16 - P DIL	
	1	5322 255 44217	IC-FOOT 40 - P DIL	
	4	5322 255 44259	IC-FOOT 20 - P DIL	
	4	5322 255 44109	IC-FOOT 24 - P DIL	
	2	5322 255 44284	IC-FOOT 22 - P DIL	
79	2	4822 502 10692	CIL BOLT M3X30X19	
80	2	4822 532 10582	Washer 3.2X9	
81	2	4822 532 60711	Insulation bush	
82	2	5322 532 50488	Washer 4.3X9	
83	2	4822 532 10582	Washer 3.2X9	
84	2	4822 505 10325	Nut M3	
85	2	4822 532 10582	Washer	
86	2	4822 530 80173	Spring washer	
87	2	4822 505 10325	Nut M3	
88	1	5322 532 24578	Bushing	
89	1	4822 530 80173	Spring washer	
90	1	4822 502 11064	CIL bolt M3X6	
91	2	5322 255 40029	Transistor socket	
92	1	5322 256 40017	Fuse holder	
93	1	5322 325 64061	Cable grommet	
94	1	5322 405 94046	Bracket	
95	1	4822 502 10693	CIL bolt M4X8	
96	1	5322 321 14066	Mains cord assy	
97	4	5322 462 44457	Foot	
98	4	5322 529 14067	Rubber puffer	
99	4	4822 502 10056	CIL bolt M4X55	
100	4	5322 532 14593	Washer 4.3X12	

Item	Qty	Order number	Description
101	4	4822 530 80163	Spring washer 4.1
102	4	5322 532 24591	Distance bushing 6X5
103	8	5322 532 24592	Distance bushing 6X20
104	1	5322 447 94639	Inner rear plate (01 version)
104	1	5322 466 80791	Inner rear plate (02 and up)
105	6	5322 532 24577	Threaded spacer
106	4	5322 381 14286	Window red
107	2	5322 532 64277	Holder
108	4	5322 532 64278	Ring
109	2	5322 532 14696	Contact ring
110	2	5322 492 64765	Contact spring
111	1	5322 447 94652	Cast. al. front panel
112	1	5322 447 94653	Cast. al. rear panel
113	4	5322 466 90998	Spacer for alphanumeric display
114	25	5322 414 25613	Push button + green (01 version)
114	25	5322 414 26415	Push button + green (02 and up)

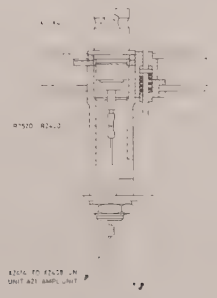
RANGE INDICATION PROBE PARTS FIG. 1.11.

FLEXIBLE COUPLINGS



12.2. ELECTRICAL PARTS

Unit	Order number	Description
A101	5322 266 21002	Connector assy.
A2	5322 216 54264	Front unit (Per order)
A201	5322 216 54265	Front board
A203	5322 216 54266	Interconn. board
A204	5322 216 54267	Display switch board
A205	5322 216 54268	Save or dl. sw. board
A206	5322 216 54269	Clear switch board
A207	5322 216 54296	Scale switch board
A4	5322 216 54272	Micro proc. unit
A6	5322 216 54273	Ram unit
A7	5322 216 54274	Buffer unit
A8	5322 216 54275	Conversion unit
A9	5322 216 54276	ACL unit
A10	5322 216 54295	CCD logic
A11	5322 216 54278	P^2CCD unit
A12	5322 216 54279	Time base unit
A13	5322 216 54281	Delay trigg. unit
A15	5322 216 54282	DC-power unit
A16	5322 216 54283	AC-power unit
A18	5322 320 44053	Delay line
A20	5322 216 54284	Final amplifier unit
A23	5322 218 64116	Multiplier assy (D3101) (inclusive cable)
	5322 263 74144	Extension card
A4011	5322 209 54684	PROM assy. (Set of 3 programmed PROM's)



UNIT A101

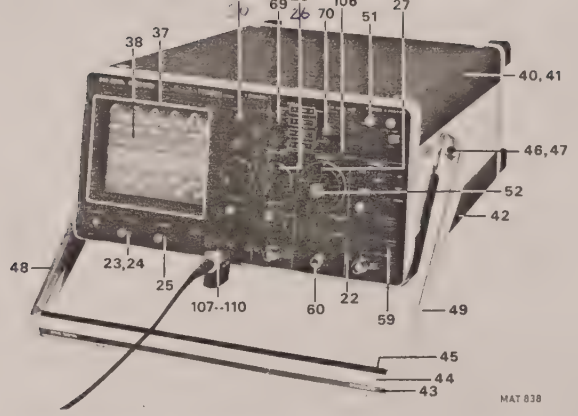


Fig. 12.1.3.

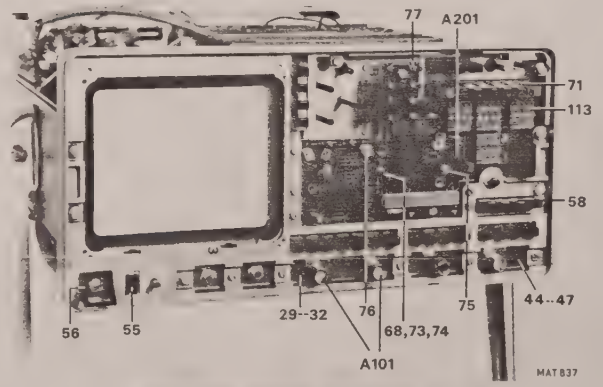


Fig. 12.1.4.

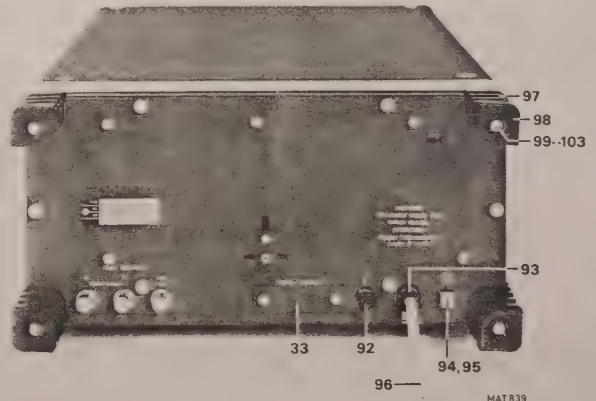


Fig. 12.1.5.

POSNR	DESCRIPTION		ORDERING CODE
C 634	33UF-10+50	16	4822 124 20688
C 636	100UF-10+50	10	4822 124 20679
C 637	10NF-20+50	100	4822 122 31414
C 638	10NF-20+50	100	4822 122 31414
C 639	10NF-20+50	100	4822 122 31414
C 641	10NF-20+50	100	4822 122 31414
C 701	10NF-20+50	100	4822 122 31414
C 702	10NF-20+50	100	4822 122 31414
C 703	10NF-20+50	100	4822 122 31414
C 704	10NF-20+50	100	4822 122 31414
C 706	10NF-20+50	100	4822 122 31414
C 707	10NF-20+50	100	4822 122 31414
C 708	10NF-20+50	100	4822 122 31414
C 709	10NF-20+50	100	4822 122 31414
C 711	10NF-20+50	100	4822 122 31414
C 712	10NF-20+50	100	4822 122 31414
C 713	10NF-20+50	100	4822 122 31414
C 714	56PF 2	100	4822 122 31521
C 716	1NF 10	100	4822 122 30027
C 717	10NF-20+50	100	4822 122 31414
C 718	10NF-20+50	100	4822 122 31414
C 719	10NF-20+50	100	4822 122 31414
C 721	10NF-20+50	100	4822 122 31414
C 722	10NF-20+50	100	4822 122 31414
C 723	10NF-20+50	100	4822 122 31414
C 724	150NF 10%	100V	5322 121 40323
C 726	330UF-10+50	10	4822 124 20684
C 801	10NF-20+50	100	4822 122 31414
C 802	10NF-20+50	100	4822 122 31414
C 803	10NF-20+50	100	4822 122 31414
C 804	10NF-20+50	100	4822 122 31414
C 806	10NF-20+50	100	4822 122 31414
C 807	10NF-20+50	100	4822 122 31414
C 808	10NF-20+50	100	4822 122 31414
C 809	10NF-20+50	100	4822 122 31414
C 811	10NF-20+50	100	4822 122 31414
C 812	10NF-20+50	100	4822 122 31414
C 813	330UF-10+50	10	4822 124 20684
C 814	10NF-20+50	100	4822 122 31414
C 816	10NF-20+50	100	4822 122 31414
C 817	10NF-20+50	100	4822 122 31414
C 818	10NF-20+50	100	4822 122 31414
C 819	10NF-20+50	100	4822 122 31414
C 821	33UF-10+50	16	4822 124 20688
C 822	10NF-20+50	100	4822 122 31414
C 823	10NF-20+50	100	4822 122 31414
C 824	33UF-10+50	16	4822 124 20688
C 826	10NF-20+50	100	4822 122 31414
C 827			5322 121 54231
C 828	10NF-20+50	100	4822 122 31414
C 829	10NF-20+50	100	4822 122 31414
C 901	10NF-20+50	100	4822 122 31414
C 902	10NF-20+50	100	4822 122 31414
C 903	10NF-20+50	100	4822 122 31414
C 904	10NF-20+50	100	4822 122 31414
C 905	470PF 10	100	4822 122 30034
C 906	10NF-20+50	100	4822 122 31414
C 907	10NF-20+50	100	4822 122 31414
C 908	10NF-20+50	100	4822 122 31414
C 909	10NF-20+50	100	4822 122 31414
C 911	1NF 10	100	4822 122 30027
C 912	10NF-20+50	100	4822 122 31414
C 913	56PF 2	100	4822 122 31521
C 914	10NF-20+50	100	4822 122 31414
C 916	150NF 10%	100V	5322 121 40323

POSNR	DESCRIPTION		ORDERING CODE
C 917	10NF-20+50	100	4822 122 31414
C 918	10NF-20+50	100	4822 122 31414
C 919	10NF-20+50	100	4822 122 31414
C 920	220PF 2	100	4822 122 31173
C 921	10NF-20+50	100	4822 122 31414
C 922	10NF-20+50	100	4822 122 31414
C 923	10NF-20+50	100	4822 122 31414
C 924	10NF-20+50	100	4822 122 31414
C 925	470PF 10	100	4822 122 30034
C 926	10NF-20+50	100	4822 122 31414
C 927	10NF-20+50	100	4822 122 31414
C 928	10NF-20+50	100	4822 122 31414
C 929	330UF-10+50	10	4822 124 20684
C 931	10NF-20+50	100	4822 122 31414
C 932	10NF-20+50	100	4822 122 31414
C 933	10NF-20+50	100	4822 122 31414
C 934	10NF-20+50	100	4822 122 31414
C 1001	15UF-10+50	40	4822 124 20709
C 1002	100PF 2	100	4822 122 31316
C 1003	10NF-20+50	100	4822 122 31414
C 1004	33PF 2	100	4822 122 31067
C 1006	33PF 2	100	4822 122 31067
C 1007	10NF-20+50	100	4822 122 31414
C 1008	10NF-20+50	100	4822 122 31414
C 1009	10NF-20+50	100	4822 122 31414
C 1010	10NF-20+50	100	4822 122 31414
C 1011	10NF-20+50	100	4822 122 31414
C 1012	22NF 10%	400V	5322 121 44232
C 1013	22NF 10%	400V	5322 121 44232
C 1014	10NF-20+50	100	4822 122 31414
C 1016	10NF-20+50	100	4822 122 31414
C 1017	10NF-20+50	100	4822 122 31414
C 1018	10NF-20+50	100	4822 122 31414
C 1019	10NF-20+50	100	4822 122 31414
C 1020	15UF-10+50	40	4822 124 20709
C 1021	10NF-20+50	100	4822 122 31414
C 1022	10NF-20+50	100	4822 122 31414
C 1023	10NF-20+50	100	4822 122 31414
C 1024	10NF-20+50	100	4822 122 31414
C 1026	10NF-20+50	100	4822 122 31414
C 1027	10NF-20+50	100	4822 122 31414
C 1028	10NF-20+50	100	4822 122 31414
C 1029	10NF-20+50	100	4822 122 31414
C 1031	68UF-10+50	16	4822 124 20689
C 1032	68UF-10+50	16	4822 124 20689
C 1033	15PF 2	100	4822 122 31058
C 1034	220PF 2	100	4822 122 31222
C 1036	220PF 2	100	4822 122 31222
C 1037	15PF 2	100	4822 122 31058
C 1038	10NF-20+50	100	4822 122 31414
C 1039	15UF 10%	16V	4822 124 20977
C 1041	10NF-20+50	100	4822 122 31414
C 1042	10NF-20+50	100	4822 122 31414
C 1043	10NF-20+50	100	4822 122 31414
C 1044	10NF-20+50	100	4822 122 31414
C 1046	100UF-10+50	10	4822 124 20679
C 1047	10UF-10+50	63	4822 124 20723
C 1048	15UF 10%	16V	4822 124 20977
C 1049	47UF-10+50	10	4822 124 20678
C 1101	10NF-20+50	100	4822 122 31414
C 1102	8,2PF 0,25PF	100	4822 122 31052
C 1103	8,2PF 0,25PF	100	4822 122 31052
C 1106	1NF 10	100	4822 122 30027

POSNR	DESCRIPTION		ORDERING CODE
C 1107	10NF-20+50	100	4822 122 31414
C 1108	10NF-20+50	100	4822 122 31414
C 1109	15UF-10+50	40	4822 124 20709
C 1110	5,6PF 0,25PF	100	4822 122 31047
C 1111	10UF-10+50	63	4822 124 20728
C 1112	10UF-10+50	63	4822 124 20728
C 1113	10NF-20+50	100	4822 122 31414
C 1114	10NF-20+50	100	4822 122 31414
C 1115	5,6PF 0,25PF	100	4822 122 31047
C 1116	10NF-20+50	100	4822 122 31414
C 1117	33UF-10+50	40	4822 124 20712
C 1118	1NF 10	100	4822 122 30027
C 1119	10NF-20+50	100	4822 122 31414
C 1121	15UF-10+50	40	4822 124 20709
C 1122	10NF-20+50	100	4822 122 31414
C 1123	10NF-20+50	100	4822 122 31414
C 1124	1NF 10	100	4822 122 30027
C 1126	1NF 10	100	4822 122 30027
C 1127	10NF-20+50	100	4822 122 31414
C 1128	8,2PF 0,25PF	100	4822 122 31052
C 1129	8,2PF 0,25PF	100	4822 122 31052
C 1131	10NF-20+50	100	4822 122 31414
C 1132	10NF-20+50	100	4822 122 31414
C 1133	15UF 10%	16V	4822 124 20977
C 1201	10NF-20+50	100	4822 122 31414
C 1202	10NF-20+50	100	4822 122 31414
C 1203	10NF-20+50	100	4822 122 31414
C 1204	10NF-20+50	100	4822 122 31414
C 1206	10NF-20+50	100	4822 122 31414
C 1207	10NF-20+50	100	4822 122 31414
C 1208	10NF-20+50	100	4822 122 31414
C 1209	10NF-20+50	100	4822 122 31414
C 1210	10NF-20+50	100	4822 122 31414
C 1211	1NF 10	100	4822 122 30027
C 1213	3,9PF 0,25PF	100	5322 122 34107
C 1214	47UF-10+50	10	4822 124 20678
C 1216	47UF-10+50	10	4822 124 20678
C 1217	10NF-20+50	100	4822 122 31414
C 1218	10NF-20+50	100	4822 122 31414
C 1219	10NF-20+50	100	4822 122 31414
C 1221	10NF-20+50	100	4822 122 31414
C 1222	10NF-20+50	100	4822 122 31414
C 1223	10NF-20+50	100	4822 122 31414
C 1224	10NF-20+50	100	4822 122 31414
C 1226	10NF-20+50	100	4822 122 31414
C 1227	10NF-20+50	100	4822 122 31414
C 1228	10NF-20+50	100	4822 122 31414
C 1229	10NF-20+50	100	4822 122 31414
C 1230	10NF-20+50	100	4822 122 31414
C 1231	10NF-20+50	100	4822 122 31414
C 1232	10NF-20+50	100	4822 122 31414
C 1233	10NF-20+50	100	4822 122 31414
C 1234	47UF-10+50	10	4822 124 20678
C 1235	10NF-20+50	100	4822 122 31414
C 1236	47UF-10+50	10	4822 124 20678
C 1237	10NF-20+50	100	4822 122 31414
C 1301	10NF-20+50	100	4822 122 31414
C 1302	10NF-20+50	100	4822 122 31414
C 1303	10NF-20+50	100	4822 122 31414
C 1304	10NF-20+50	100	4822 122 31414
C 1306	10NF-20+50	100	4822 122 31414
C 1307	10NF-20+50	100	4822 122 31414
C 1308	10NF-20+50	100	4822 122 31414
C 1309	10NF-20+50	100	4822 122 31414
C 1311	10NF-20+50	100	4822 122 31414

POSNR	DESCRIPTION	ORDERING CODE
C 1312	10NF-20+50 100	4822 122 31414
C 1313	10NF-20+50 100	4822 122 31414
C 1314	47UF-10+50 10	4822 124 20678
C 1316	47UF-10+50 10	4822 124 20678
C 1317	1NF 1% 630V	4822 121 50591
C 1318	10NF-20+50 100	4822 122 31414
C 1319	33UF-10+50 16	4822 124 20688
C 1321	10NF-20+50 100	4822 122 31414
C 1322	10NF-20+50 100	4822 122 31414
C 1323	10NF-20+50 100	4822 122 31414
C 1324	10NF-20+50 100	4822 122 31414
C 1326	1NF 10 100	4822 122 30027
C 1327	1NF 1% 630V	4822 121 50591
C 1328	150NF 10% 100V	5322 121 40323
C 1329	33UF-10+50 16	4822 124 20688
C 1331	56PF 2 100	4822 122 31521
C 1332	10NF-20+50 100	4822 122 31414
C 1333	10UF-10+50 63	4822 124 20728
C 1334	100PF 2 100	4822 122 31504
C 1501	47NF 10% 250V	5322 121 44138
C 1502	15NF 10% 1600V	4822 121 40123
C 1503	15NF 10% 1600V	4822 121 40123
C 1504	470PF 10% 2KV	5322 122 54019
C 1506	470PF 20% 4KV	5322 122 54004
C 1507	10UF-10+50 63	4822 124 20728
C 1508	47UF-10+50 63	4822 124 20733
C 1509	330UF-10+50 10	4822 124 20684
C 1511	330UF-10+50 10	4822 124 20684
C 1512	1000UF-10+50 25	4822 124 20786
C 1513	1000UF-10+50 25	4822 124 20786
C 1514	100PF 2 100	4822 122 31504
C 1516	100PF 2 100	4822 122 31504
C 1517	68NF 10% 630V	4822 121 40279
C 1518	470PF 10% 2KV	5322 122 54019
C 1519	68NF 10% 630V	4822 121 40279
C 1521	470PF 10% 2KV	5322 122 54019
C 1522	470PF 10% 2KV	5322 122 54019
C 1523	150NF 10% 400V	5322 121 40307
C 1524	150NF 10% 400V	5322 121 40307
C 1526	2200UF-10+50 10	4822 124 20771
C 1527	2200UF-10+50 10	4822 124 20771
C 1528	33UF-10+50 16	4822 124 20688
C 1529	150NF 10% 400V	5322 121 40307
C 1531	150NF 10% 400V	5322 121 40307
C 1532	150NF 10% 100V	5322 121 40323
C 1533	10UF-10+50 63	4822 124 20728
C 1534	33UF-10+50 16	4822 124 20688
C 1536	47UF-10+50 10	4822 124 20678
C 1537	1UF 10% 100V	5322 121 40197
C 1538	68NF 10% 250V	5322 121 44137
C 1539	10NF-20+50 100	4822 122 31414
C 1541	10NF 10% 630V	5322 121 44201
C 1542	1UF 10% 100V	5322 121 40197
C 1543	33NF 10% 400V	5322 121 44025
C 1544	12PF 2 100	4822 122 31056
C 1546	150NF 10% 100V	5322 121 40323
C 1547	100NF 10% 100V	4822 121 40231
C 1548	68NF 10% 250V	5322 121 44137
C 1549	560PF 10 100	4822 122 30126
C 1551	560PF 10 100	4822 122 30126
C 1552	330UF-10+50 10	4822 124 20684
C 1553	10UF-10+50 63	4822 124 20728
C 1554	100NF 10% 100V	4822 121 40231
C 1555	1NF 10 100	4822 122 30027
C 1556	10NF-20+50 100	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 1557	10NF-20+50	100	4822 122 31414
C 1558	10NF-20+50	100	4822 122 31414
C 1601	68NF 10%	630V	4822 121 40279
C 1602			5322 121 44333
C 1603			5322 121 44333
C 1604	220UF-10+50	350	5322 124 44007
C 1606	220UF-10+50	350	5322 124 44007
C 1607	270PF 10%	2KV	5322 122 54024
C 1608	220NF 10%	250V	5322 121 44142
C 1609	10UF-10+50	63	4822 124 20728
C 1610	1,8NF 10	100	4822 122 30048
C 1611	10UF-10+50	63	4822 124 20728
C 1612	220NF 10%	100V	4822 121 40232
C 1613	22NF 10%	400V	5322 121 44232
C 1614	22NF 10%	400V	5322 121 44232
C 1616	150NF 10%	100V	5322 121 40323
C 1617	2,2NF 10	100	4822 122 30114
C 1618	68NF 10%	250V	5322 121 44137
C 1620	470PF 10%	2KV	5322 122 54019
C 1621	10UF-10+50	63	4822 124 20728
C 1622	22UF-10+50	25	4822 124 20698
C 1623	22UF-10+50	25	4822 124 20698
C 1624	1NF 10	100	4822 122 30027
C 1625	470PF 10%	2KV	5322 122 54019
C 1701	100NF 10%	250V	4822 121 40036
C 1702	100NF 10%	250V	4822 121 40036
C 2001	10NF-20+50	100	4822 122 31414
C 2002	10NF-20+50	100	4822 122 31414
C 2003	10NF-20+50	100	4822 122 31414
C 2004	10NF-20+50	100	4822 122 31414
C 2006	10NF-20+50	100	4822 122 31414
C 2007	1NF 1%	630V	4822 121 50591
C 2008	220PF 2	100	4822 122 31173
C 2009	10NF-20+50	100	4822 122 31414
C 201	10NF-20+50	100	4822 122 31414
C 2011	10NF-20+50	100	4822 122 31414
C 2012	10NF-20+50	100	4822 122 31414
C 2013	10NF-20+50	100	4822 122 31414
C 2014			5322 121 54229
C 2016	10NF-20+50	100	4822 122 31414
C 2017	10NF-20+50	100	4822 122 31414
C 2018	10NF-20+50	100	4822 122 31414
C 2019	10NF-20+50	100	4822 122 31414
C 202	10NF-20+50	100	4822 122 31414
C 2021	10NF-20+50	100	4822 122 31414
C 2022	10NF-20+50	100	4822 122 31414
C 2023	10NF-20+50	100	4822 122 31414
C 2024	10NF-20+50	100	4822 122 31414
C 2026	10NF-20+50	100	4822 122 31414
C 2027			5322 121 54229
C 2028			5322 121 54229
C 2029	10NF-20+50	100	4822 122 31414
C 203	10NF-20+50	100	4822 122 31414
C 2030	82PF 2	100	5322 122 31577
C 2031	10NF-20+50	100	4822 122 31414
C 2032	10NF-20+50	100	4822 122 31414
C 2033	68NF 10%	250V	5322 121 44137
C 2034	10NF-20+50	100	4822 122 31414
C 2036	33UF-10+50	16	4822 124 20688
C 2037	33UF-10+50	16	4822 124 20688
C 2038	220NF 10%	100V	4822 121 40232
C 2039	68NF 10%	250V	5322 121 44137
C 204	10NF-20+50	100	4822 122 31414
C 2041			5322 121 54229
C 2042	10NF-20+50	100	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 2043			5322 121 54229
C 206	10NF-20+50	100	4822 122 31414
C 207	47UF-10+50	10	4822 124 20678
C 2400	47UF-10+50	10	4822 124 20678
C 2401	10NF-20+50	100	4822 122 31414
C 2402	10NF-20+50	100	4822 122 31414
C 2403	10NF-20+50	100	4822 122 31414
C 2404	10NF-20+50	100	4822 122 31414
C 2405	1,5PF 0,25PF	100	4822 122 30105
C 2406	10NF-20+50	100	4822 122 31414
C 2407	22PF 2	100	4822 122 31063
C 2408	10NF-20+50	100	4822 122 31414
C 2409	5,5PF		5322 125 54027
C 241	10NF-20+50	100	4822 122 31414
C 2410	3,9PF 0,25PF	500	4822 122 31217
C 2411	10NF-20+50	100	4822 122 31414
C 2412	10NF-20+50	100	4822 122 31414
C 2413	300PF 10	300	5322 123 10168
C 2414	22NF 10%	250V	4822 121 40407
C 2415	10NF-20+50	100	4822 122 31414
C 2416	3PF		5322 125 54026
C 2417	10NF-20+50	100	4822 122 31414
C 2418	10NF-20+50	100	4822 122 31414
C 2419	10NF-20+50	100	4822 122 31414
C 242	10NF-20+50	100	4822 122 31414
C 2420	10NF-20+50	100	4822 122 31414
C 2421	10NF-20+50	100	4822 122 31414
C 2422	10NF-20+50	100	4822 122 31414
C 2423	22PF 2	100	4822 122 31063
C 2424	18PF		5322 125 50051
C 2425	10NF-20+50	100	4822 122 31414
C 2426	10NF-20+50	100	4822 122 31414
C 2427	5,5PF		5322 125 54027
C 2428	560PF 10	500	4822 122 31166
C 2429	10NF-20+50	100	4822 122 31414
C 243	10NF-20+50	100	4822 122 31414
C 2430	470PF 10	100	4822 122 30034
C 2431	68PF 2	500	4822 122 31207
C 2432	10NF-20+50	100	4822 122 31414
C 2433	10NF-20+50	100	4822 122 31414
C 2434	10NF-20+50	100	4822 122 31414
C 2435	10NF-20+50	100	4822 122 31414
C 2436	1NF 10	100	4822 122 30027
C 2437	1,5PF 0,25PF	100	4822 122 30105
C 2438	10NF-20+50	100	4822 122 31414
C 2439	39PF 2	100	4822 122 31069
C 244	10NF-20+50	100	4822 122 31414
C 2440	10NF-20+50	100	4822 122 31414
C 2441	39PF 2	100	4822 122 31069
C 2442	5,5PF		5322 125 54027
C 2443	30PF 10	300	5322 123 34001
C 2444	3PF		5322 125 54026
C 2445	2,2PF 0,25PF	500	4822 122 31186
C 2446	470PF 10	100	4822 122 30034
C 2447	18PF		5322 125 50051
C 2448	10NF-20+50	100	4822 122 31414
C 2449	2,2PF 0,25PF	100	4822 122 31036
C 2450	2,2PF 0,25PF	100	4822 122 31036
C 2451	10NF-20+50	100	4822 122 31414
C 2452	10NF-20+50	100	4822 122 31414
C 2453	10NF-20+50	100	4822 122 31414
C 2454	10PF 2	100	4822 122 31054
C 2455	10NF-20+50	100	4822 122 31414
C 2456	22PF 2	100	4822 122 31063
C 2457	10NF-20+50	100	4822 122 31414

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C 2458	10NF-20+50	100	4822 122 31414
C 2459	22PF 2	100	4822 122 31063
C 246	10NF-20+50	100	4822 122 31414
C 2460	10NF-20+50	100	4822 122 31414
C 2461	10NF-20+50	100	4822 122 31414
C 2462	10NF-20+50	100	4822 122 31414
C 2463	10NF-20+50	100	4822 122 31414
C 2464	10NF-20+50	100	4822 122 31414
C 2465	10NF-20+50	100	4822 122 31414
C 2466	10NF-20+50	100	4822 122 31414
C 2467	150NF 10%	100V	5322 121 40323
C 2468	10NF-20+50	100	4822 122 31414
C 2469	10NF-20+50	100	4822 122 31414
C 247	10NF-20+50	100	4822 122 31414
C 2470	1,5PF 0,25PF	100	4822 122 30105
C 2471	10NF-20+50	100	4822 122 31414
C 2472	10NF-20+50	100	4822 122 31414
C 2473	22PF 2	100	4822 122 31063
C 2474	10NF-20+50	100	4822 122 31414
C 2475	3,9PF 0,25PF	500	4822 122 31217
C 2476	22NF 10%	250V	4822 121 40407
C 2477	5,5PF		5322 125 54027
C 2478	10NF-20+50	100	4822 122 31414
C 2479	10NF-20+50	100	4822 122 31414
C 248	10NF-20+50	100	4822 122 31414
C 2480	10NF-20+50	100	4822 122 31414
C 2481	10NF-20+50	100	4822 122 31414
C 2482	10NF-20+50	100	4822 122 31414
C 2483	300PF 10	300	5322 123 10168
C 2484	3PF		5322 125 54026
C 2485	10NF-20+50	100	4822 122 31414
C 2486	10NF-20+50	100	4822 122 31414
C 2487	10NF-20+50	100	4822 122 31414
C 2488	10NF-20+50	100	4822 122 31414
C 2489	10NF-20+50	100	4822 122 31414
C 249	10NF-20+50	100	4822 122 31414
C 2490	22PF 2	100	4822 122 31063
C 2491	10NF-20+50	100	4822 122 31414
C 2492	10NF-20+50	100	4822 122 31414
C 2495	10NF-20+50	100	4822 122 31414
C 2496	18PF		5322 125 50051
C 2497	10NF-20+50	100	4822 122 31414
C 2498	10NF-20+50	100	4822 122 31414
C 2499	22PF 2	100	4822 122 31063
C 2501	220UF-10+50	16	4822 124 20693
C 2502	220UF-10+50	16	4822 124 20693
C 2503	5,5PF		5322 125 54027
C 2504	560PF 10	500	4822 122 31166
C 2506	10NF-20+50	100	4822 122 31414
C 2507	68PF 2	500	4822 122 31207
C 2508	10NF-20+50	100	4822 122 31414
C 2509	10NF-20+50	100	4822 122 31414
C 251	10NF-20+50	100	4822 122 31414
C 2510	470PF 10	100	4822 122 30034
C 2511	10NF-20+50	100	4822 122 31414
C 2512	1NF 10	100	4822 122 30027
C 2513	1,5PF 0,25PF	100	4822 122 30105
C 2514	10NF-20+50	100	4822 122 31414
C 2515	2,2PF 0,25PF	500	4822 122 31186
C 2516	39PF 2	100	4822 122 31069
C 2517	39PF 2	100	4822 122 31069
C 2518	5,5PF		5322 125 54027
C 2519	30PF 10	300	5322 123 34001
C 252	330UF-10+50	10	4822 124 20684
C 2520	10NF-20+50	100	4822 122 31414

POSNR	DESCRIPTION		ORDERING CODE
C 2521	3PF		5322 125 54026
C 2522	470PF 10	100	4822 122 30034
C 2523	18PF		5322 125 50051
C 2524	10NF-20+50	100	4822 122 31414
C 2525	10NF-20+50	100	4822 122 31414
C 2526	10NF-20+50	100	4822 122 31414
C 2527	10NF-20+50	100	4822 122 31414
C 2528	10PF 2	100	4822 122 31054
C 2529	10NF-20+50	100	4822 122 31414
C 253	47UF-10+50	10	4822 124 20678
C 2530	10NF-20+50	100	4822 122 31414
C 2531	10NF-20+50	100	4822 122 31414
C 2532	22PF 2	100	4822 122 31063
C 2533	10NF-20+50	100	4822 122 31414
C 2534	10NF-20+50	100	4822 122 31414
C 2535	33UF-10+50	16	4822 124 20688
C 2536	10NF-20+50	100	4822 122 31414
C 2537	10NF-20+50	100	4822 122 31414
C 2538	10NF-20+50	100	4822 122 31414
C 2539	220UF-10+50	16	4822 124 20693
C 254	10NF-20+50	100	4822 122 31414
C 2540	680UF-10+50	16	4822 124 20776
C 2541	10NF-20+50	100	4822 122 31414
C 2542	10NF-20+50	100	4822 122 31414
C 2543	220UF-10+50	16	4822 124 20693
C 2544	10NF-20+50	100	4822 122 31414
C 2545	100UF-10+50	10	4822 124 20679
C 2546	10NF-20+50	100	4822 122 31414
C 2547	10NF-20+50	100	4822 122 31414
C 2548	10NF-20+50	100	4822 122 31414
C 2549	100UF-10+50	10	4822 124 20679
C 2550	47UF-10+50	10	4822 124 20678
C 2551	10NF-20+50	100	4822 122 31414
C 2552	10NF-20+50	100	4822 122 31414
C 2553	10NF-20+50	100	4822 122 31414
C 2554	10NF-20+50	100	4822 122 31414
C 2555	10NF-20+50	100	4822 122 31414
C 2556	10NF-20+50	100	4822 122 31414
C 2557	10NF-20+50	100	4822 122 31414
C 2558	10NF-20+50	100	4822 122 31414
C 2559	10NF-20+50	100	4822 122 31414
C 256	33UF-10+50	16	4822 124 20688
C 2560	10NF-20+50	100	4822 122 31414
C 2561	10NF-20+50	100	4822 122 31414
C 2562	10NF-20+50	100	4822 122 31414
C 2563	10NF-20+50	100	4822 122 31414
C 2564	10NF-20+50	100	4822 122 31414
C 2566	10NF-20+50	100	4822 122 31414
C 2567	10NF-20+50	100	4822 122 31414
C 2568	3,3UF 40%	16V	4822 124 20947
C 2569	10NF-20+50	100	4822 122 31414
C 257	33UF-10+50	16	4822 124 20688
C 2570	10NF-20+50	100	4822 122 31414
C 2571	10NF-20+50	100	4822 122 31414
C 2572	10NF-20+50	100	4822 122 31414
C 2573	10NF-20+50	100	4822 122 31414
C 2574	10NF-20+50	100	4822 122 31414
C 2575	10NF-20+50	100	4822 122 31414
C 2576	10NF-20+50	100	4822 122 31414
C 2577	2,2NF 10	100	4822 122 30114
C 2578	2,2NF 10	100	4822 122 30114
C 2579	2,2NF 10	100	4822 122 30114
C 258	33UF-10+50	16	4822 124 20688
C 2580	2,2NF 10	100	4822 122 30114
C 2583	6,8PF 0,25PF	100	4822 122 31049

POSNR	DESCRIPTION		ORDERING CODE
C 2584	6,8PF 0,25PF	100	4822 122 31049
C 2585	6,8PF 0,25PF	100	4822 122 31049
C 2586	6,8PF 0,25PF	100	4822 122 31049
C 2587	10NF-20+50	100	4822 122 31414
C 2588	10NF-20+50	100	4822 122 31414
C 2589	10NF-20+50	100	4822 122 31414
C 2590	10NF-20+50	100	4822 122 31414
C 2701	10NF-20+50	100	4822 122 31414
C 2702	10NF-20+50	100	4822 122 31414
C 2703	47UF-10+50	10	4822 124 20678
C 2704	82PF 2	100	4822 122 31243
C 2705	10NF-20+50	100	4822 122 31414
C 2706	8,2PF 0,25PF	500	4822 122 31194
C 2707	6,8PF 0,25PF	500	4822 122 31192
C 2708	100PF 2	500	5322 122 31626
C 2709	4,7UF-10+50	63	5322 124 24211
C 2710	33UF-10+50	16	4822 124 20688
C 2711	220NF 10%	100V	4822 121 40232
C 2712	33UF-10+50	16	4822 124 20688
C 2713	10NF-20+50	100	4822 122 31414
C 2714	4,7NF 10	100	4822 122 30128
C 2715	15PF 2	100	4822 122 31058
C 2716	1NF 10	100	4822 122 30027
C 2717	10NF-20+50	100	4822 122 31414
C 2718	68PF 2	100	4822 122 31349
C 2719	22NF 10%	400V	5322 121 44232
C 2721	180PF 2	100	5322 122 34144
C 2722	47UF-10+50	10	4822 124 20678
C 2723	33UF-10+50	16	4822 124 20688
C 2724	12PF 2	500	4822 122 31196
C 2726	10NF-20+50	100	4822 122 31414
C 2727	1NF 10	100	4822 122 30027
C 2728	10NF-20+50	100	4822 122 31414
C 2729	270PF 2	100	4822 122 31335
C 2730	22PF 2	100	4822 122 31063
C 2731	10NF-20+50	100	4822 122 31414
C 2732	10NF-20+50	100	4822 122 31414
C 2733	47UF-10+50	10	4822 124 20678
C 2734	220NF 10%	100V	4822 121 40232
C 2736	33UF-10+50	16	4822 124 20688
C 2737	680NF 10%	100V	5322 121 40233
C 2738	100PF 2	100	4822 122 31316
C 2739	10NF-20+50	100	4822 122 31414
C 2741	33UF-10+50	16	4822 124 20688
C 2742	10NF-20+50	100	4822 122 31414
C 2743	680NF 10%	100V	5322 121 40233
C 2744	10NF-20+50	100	4822 122 31414
C 2745	2,2PF 0,25PF	100	4822 122 31036
C 2746	100PF 2	100	4822 122 31316
C 2747	10NF-20+50	100	4822 122 31414
C 2748	10NF-20+50	100	4822 122 31414
C 2749	10NF-20+50	100	4822 122 31414
C 2750	10NF-20+50	100	4822 122 31414
C 2751	10NF-20+50	100	4822 122 31414
C 2752	10NF-20+50	100	4822 122 31414
C 2753	10NF-20+50	100	4822 122 31414
C 2754	10NF-20+50	100	4822 122 31414
C 2756	10NF-20+50	100	4822 122 31414
C 2757	10NF-20+50	100	4822 122 31414
C 2901	6SUF-10+50	16	4822 124 20689
C 2902	47UF-10+50	10	4822 124 20678
C 2903	47UF-10+50	10	4822 124 20678
C 2904	10UF-10+50	63	4822 124 20728
C 2905	10NF-20+50	100	4822 122 31414
C 2906	47UF-10+50	10	4822 124 20678

POSNR	DESCRIPTION			ORDERING CODE
C 2907	47UF-10+50	10	4822 124 20678	
C 2908	33UF-10+50	16	4822 124 20688	
C 2909	33UF-10+50	16	4822 124 20688	
C 2911	10NF-20+50	100	4822 122 31414	
C 2912	10NF-20+50	100	4822 122 31414	
C 2913	12PF	2	100	4822 122 31056
C 2914	100PF	2	100	4822 122 31316
C 2916	12PF	2	100	4822 122 31056
C 2917	1NF	10	100	4822 122 30027
C 2918	220PF	2	100	4822 122 31222
C 2919	4,7NF	10	100	4822 122 30128
C 2920	10NF-20+50		100	4822 122 31414
C 2921	5,6PF 0,25PF		100	4822 122 31047
C 2922	10NF-20+50		100	4822 122 31414
C 2923				5322 121 54228
C 2924	1NF	10	100	4822 122 30027
C 2925	4,7NF	10	100	4822 122 30128
C 2926	10NF-20+50		100	4822 122 31414
C 2927	100PF	2	100	4822 122 31316
C 2928	10NF-20+50		100	4822 122 31414
C 2929	10NF-20+50		100	4822 122 31414
C 2930	1NF	10	100	4822 122 30027
C 2931	10NF-20+50		100	4822 122 31414
C 2932	1PF 0,25PF		100	4822 122 30104
C 2933	1PF 0,25PF		100	4822 122 30104
C 2934	10NF-20+50		100	4822 122 31414
C 2935	33UF 40%		10V	4822 124 20945
C 2936	10NF-20+50		100	4822 122 31414
C 2937	10NF-20+50		100	4822 122 31414
C 2938	4,7PF 0,25PF		100	4822 122 31045
C 2939	4,7PF 0,25PF		100	4822 122 31045
C 2940	10NF-20+50		100	4822 122 31414
C 2941	10NF-20+50		100	4822 122 31414
C 2942	4,7PF 0,25PF		100	4822 122 31045
C 2943	10NF-20+50		100	4822 122 31414
C 2944	10NF-20+50		100	4822 122 31414
C 2945	180PF	10	100	4822 122 30113
C 2946	33UF-10+50		16	4822 124 20688
C 2947	150NF 10%		100V	5322 121 40323
C 2948	27PF	2	100	4822 122 30045
C 3004	10NF-20+50		100	4822 122 31414
C 3005	10NF-20+50		100	4822 122 31414
C 3006	22PF	2	100	4822 122 31063
C 3007	3,9PF 0,25PF		100	5322 122 34107
C 3008	3,9PF 0,25PF		100	5322 122 34107
C 3009	470NF 10%		100V	5322 121 40175
C 3010	47UF-10+50		10	4822 124 20678
C 3011	47PF	2	100	4822 122 31072
C 3012	10NF-20+50		100	4822 122 31414
C 3013	10NF-20+50		100	4822 122 31414
C 3015	3,3UF 40%		16V	4822 124 20947
C 3016	15PF	2	100	4822 122 31058
C 3017	18PF			5322 125 50051
C 3019	12PF	2	100	4822 122 31056
C 3020	3,3UF 40%		16V	4822 124 20947
C 3021	33UF-10+50		16	4822 124 20688
C 3022	6,8UF 20%		16V	5322 124 14069
C 3023	33UF-10+50		16	4822 124 20688
C 3024	4,7NF	10	100	4822 122 30128
C 3025	100PF	2	100	4822 122 31316
C 3026	15PF	2	100	4822 122 31058
C 3027	10NF-20+50		100	4822 122 31414
C 3028	10PF	2	100	4822 122 31054
C 3029	10PF	2	100	4822 122 31054

POSNR	DESCRIPTION	ORDERING CODE
D 401	MCM51L01P45	5322 209 10155
D 402	MCM51L01P45	5322 209 10155
D 403	D2716	5322 209 50018
D 404	D2716	5322 209 50018
D 406	D2716	5322 209 50018
D 408	P8085-AH	5322 209 50032
D 409	N74LS74AN	4822 209 80782
D 411	N74LS30N	5322 209 84985
D 412	N74LS30N	5322 209 84985
D 413	SN74LS373N-00	5322 209 86062
D 414	SN74LS373N-00	5322 209 86062
D 416	SN74LS373N-00	5322 209 86062
D 417	SN74LS245N-00	5322 209 86225
D 418	N74LS138N	5322 209 85647
D 419	N74LS139N	5322 209 85839
D 421	N74LS32N	5322 209 85311
D 422	N74LS04N	5322 209 85486
D 423	N74LS74AN	4822 209 80782
D 424	HEF4528BP	5322 209 14191
D 426	HEF4093BP	5322 209 14186
D 428	N74LS04N	5322 209 85486
D 429	N74LS74AN	4822 209 80782
D 601	MCM51L01P45	5322 209 10155
D 602	MCM51L01P45	5322 209 10155
D 603	MCM51L01P45	5322 209 10155
D 604	MCM51L01P45	5322 209 10155
D 606	MCM51L01P45	5322 209 10155
D 607	MCM51L01P45	5322 209 10155
D 608	MCM51L01P45	5322 209 10155
D 609	MCM51L01P45	5322 209 10155
D 611	SN74LS257N-00	5322 209 80859
D 612	SN74LS257N-00	5322 209 80859
D 613	SN74LS373N-00	5322 209 86062
D 614	SN74LS244N-00	5322 209 86017
D 616	SN74LS244N-00	5322 209 86017
D 617	SN74LS244N-00	5322 209 86017
D 618	N74LS266N	5322 209 86163
D 619	N74LS266N	5322 209 86163
D 621	NE5018N	5322 209 86421
D 622	NE5018N	5322 209 86421
D 623	N74LS86N	5322 209 84997
D 624	N74LS86N	5322 209 84997
D 626	N74LS04N	5322 209 85486
D 627	N74LS00N	5322 209 84823
D 628	N74LS153N	5322 209 85488
D 629	N74LS02N	5322 209 85312
D 701	HEF4731VP	5322 209 14859
D 702	HEF4731VP	5322 209 14859
D 703	HEF4731VP	5322 209 14859
D 704	HEF4731VP	5322 209 14859
D 706	HEF4731VP	5322 209 14859
D 707	HEF4731VP	5322 209 14859
D 708	HEF4731VP	5322 209 14859
D 709	HEF4731VP	5322 209 14859
D 711	HEF4731VP	5322 209 14859
D 712	HEF4503BP	5322 209 14559
D 713	HEF4503BP	5322 209 14559
D 714	NE5018N	5322 209 86421
D 716	HEF40097BP	5322 209 14433
D 717	HEF40097BP	5322 209 14433
D 718	HEF4001BP	5322 209 14045

POSNR	DESCRIPTION	ORDERING CODE
D 719	HEF4049BP	5322 209 14049
D 801	HEF40S1BP	5322 209 14054
D 802	HEF4070BP	5322 209 14073
D 803	HEF4008BP	5322 209 14214
D 804	HEF4008BP	5322 209 14214
D 806	HEF4539BP	5322 209 14442
D 807	HEF4539BP	5322 209 14442
D 808	HEF4073BP	5322 209 14066
D 809	HEF4070BP	5322 209 14073
D 811	HEF40097BP	5322 209 14433
D 812	HEF40097BP	5322 209 14433
D 813	HEF40S1BP	5322 209 14054
D 814	HEF4070BP	5322 209 14073
D 816	HEF4008BP	5322 209 14214
D 817	HEF4539BP	5322 209 14442
D 818	HEF4539BP	5322 209 14442
D 819	HEF4508BP	5322 209 14559
D 821	ADC80-AGZ-10	5322 209 86447
D 822	NE5537H	5322 209 86444
D 901	N74LS153N	5322 209 85488
D 902	N74LS74AN	4822 209 80782
D 903	N74LS00N	5322 209 84823
D 904	NE5018N	5322 209 86421
D 906	N74LS08N	5322 209 84995
D 907	N74LS74AN	4822 209 80782
D 908	N74LS74AN	4822 209 80782
D 909	N74LS74AN	4822 209 80782
D 911	N74LS153N	5322 209 85488
D 912	N74LS11N	5322 209 85604
D 913	N74LS74AN	4822 209 80782
D 914	N74S00N	5322 209 84167
D 916	N74LS153N	5322 209 85488
D 917	N74LS163AN	5322 209 85863
D 918	N74LS163AN	5322 209 85863
D 919	N74LS04N	5322 209 85436
D 921	N74LS153N	5322 209 85488
D 922	N74LS00N	5322 209 84823
D 923	N74LS42N	4822 209 80936
D 924	N74LS74AN	4822 209 80782
D 926	N74LS153N	5322 209 85488
D 927	N74LS74AN	4822 209 80782
D 928	N74LS163AN	5322 209 85863
D 1001	DRIVER	5322 209 86489
D 1002	LM358N	4822 209 80818
D 1003	GXB10231P	5322 209 86003
D 1004	GXB10102P	5322 209 85955
D 1006	GXB10231P	5322 209 86003
D 1007	GXB10102P	5322 209 85955
D 1008	HEF4052BP	5322 209 14233
D 1009	LF356N	5322 209 86451
D 1011	LF356N	5322 209 86451
D 1012	GXB10125P	5322 209 86119
D 1013	GXB10124P	5322 209 86341
D 1014	GXB10231P	5322 209 86003
D 1016	LM358N	4822 209 80818
D 1017	LF356N	5322 209 86451
D 1018	HEF4052BP	5322 209 14233
D 1019	HEF4052BP	5322 209 14233
D 1021	LM7805CT	5322 209 86445
D 1102	LM358N	4822 209 80818
D 1201	HEF4526BP	5322 209 14858
D 1202	HEF4526BP	5322 209 14858
D 1203	HEF4518BP	5322 209 14064
D 1204	HEF4518BP	5322 209 14064
D 1206	HEF4518BP	5322 209 14064

POSNR	DESCRIPTION	ORDERING CODE
D 1207	HEF4520BP	5322 209 14189
D 1208	N74LS90N	5322 209 85255
D 1209	SN74S196N-00	5322 209 85411
D 1211	HEF4013BP	5322 209 10002
D 1212	UA741CN	4822 209 80617
D 1213	11C58PC	5322 209 86446
D 1214	HEF4051BP	5322 209 14212
D 1216	N74LS139N	5322 209 85839
D 1217	N74LS02N	5322 209 85312
D 1218	N74LS00N	5322 209 84823
D 1219	N74LS153N	5322 209 85488
D 1221	SN74LS373N-00	5322 209 86062
D 1222	N74LS74AN	4822 209 80782
D 1223	N74S153N	5322 209 85688
D 1224	GXB10174P	5322 209 86442
D 1226	GXB10124P	5322 209 86341
D 1227	GXB10231P	5322 209 86003
D 1228	N74LS04N	5322 209 85486
D 1229	N7404N	5322 209 86326
D 1231	GXB10125P	5322 209 86119
D 1301	N74LS191N	5322 209 84989
D 1302	N74LS191N	5322 209 84989
D 1303	GXB10124P	5322 209 86341
D 1304	GXB10231P	5322 209 86003
D 1306	GXB10137P	5322 209 86265
D 1307	GXB10125P	5322 209 86119
D 1308	SN74197N-00	5322 209 84516
D 1309	N74LS193N	5322 209 85405
D 1311	N74LS193N	5322 209 85405
D 1312	N74LS193N	5322 209 85405
D 1313	N74LS08N	5322 209 84995
D 1314	N74LS74AN	4822 209 80782
D 1316	N74LS08N	5322 209 84995
D 1317	N74LS74AN	4822 209 80782
D 1318	N74LS00N	5322 209 84823
D 1319	UA741CN	4822 209 80617
D 1321	SN74LS123N-00	5322 209 85266
D 1322	N74LS107N	5322 209 85816
D 1323	N74LS10N	5322 209 84996
D 1324	SN74LS27N-00	5322 209 86076
D 1326	SN74LS373N-00	5322 209 86062
D 1327	NE5018N	5322 209 86421
D 1328	NE5537H	5322 209 86444
D 1329	NE5537H	5322 209 86444
D 1331	UA741CN	4822 209 80617
D 1501	7905CU	5322 130 44843
D 1502	UA741CN	4822 209 80617
D 1503	UA741CN	4822 209 80617
D 1601	TDA1060	5322 209 85662
D 1602	H11A550	5322 130 94015
D 2001	LF356N	5322 209 86451
D 2002	LM358N	4822 209 80818
D 2003	LF356N	5322 209 86451
D 2004	TL082CP	5322 209 86064
D 2006	HEF4052BP	5322 209 14233
D 2007	LF356N	5322 209 86451
D 2008	HEF4053BP	5322 209 14121
D 2009	TL082CP	5322 209 86064
D 201	SN74LS373N-00	5322 209 86062
D 2011	HEF4052BP	5322 209 14233
D 2012	HEF4052BP	5322 209 14233
D 2013	HEF4052BP	5322 209 14233
D 2014	TL082CP	5322 209 86064
D 2016	TL082CP	5322 209 86064
D 2017	HEF4052BP	5322 209 14233

POSNR	DESCRIPTION	ORDERING CODE
D 2018	HEF4052BP	5322 209 14233
D 2019	NE5537H	5322 209 86444
D 202	SN74LS373N-00	5322 209 86062
D 2021	LF356N	5322 209 86451
D 2022	N74LS00N	5322 209 84823
D 2023	OQ-0017	5322 209 85627
D 2024	NE5537H	5322 209 86444
D 2026	NE5537H	5322 209 86444
D 203	N74LS138N	5322 209 85647
D 204	TDA3081	5322 209 85767
D 206	N74LS00N	5322 209 84823
D 2401	SD5000N	5322 209 85748
D 2402	N7406N	5322 209 86327
D 2403	SD5000N	5322 209 85748
D 2404	OQ 0012	5322 209 85484
D 2406	OQ 0043	5322 209 86488
D 2407	LM308AN	5322 209 86056
D 2408	LM308AN	5322 209 86056
D 2409	OQ 0012	5322 209 85484
D 241	SN74LS257N-00	5322 209 80859
D 2411	SD5000N	5322 209 85748
D 2412	OQ 0012	5322 209 85484
D 2413	OQ 0043	5322 209 86488
D 2414	LM308AN	5322 209 86056
D 2416	LM308AN	5322 209 86056
D 2417	LM339AN	4822 209 80631
D 2418	SN74LS257N-00	5322 209 80859
D 2419	SN74LS257N-00	5322 209 80859
D 242	SN74LS257N-00	5322 209 80859
D 2421	LM324N	4822 209 80587
D 2422	LM324N	4822 209 80587
D 2423	N74LS32N	5322 209 85311
D 2424	SN74LS373N-00	5322 209 86062
D 2426	SN74LS373N-00	5322 209 86062
D 2427	SN74LS373N-00	5322 209 86062
D 2428	N74LS00N	5322 209 84823
D 2429	N74LS00N	5322 209 84823
D 243	SN74LS257N-00	5322 209 80859
D 2431	N74LS139N	5322 209 85839
D 2432	SN74LS27N-00	5322 209 86076
D 244	N74LS08N	5322 209 84995
D 246	N74LS138N	5322 209 85647
D 247	SN74LS257N-00	5322 209 80859
D 248	SN74LS257N-00	5322 209 80859
D 249	SN74LS257N-00	5322 209 80859
D 2701	HEF4052BP	5322 209 14233
D 2702	SN74LS123N-00	5322 209 85266
D 2703	CA3086	5322 209 86236
D 2704	LM358N	4822 209 80818
D 2707	N74LS74AN	4822 209 80782
D 2708	LF356N	5322 209 86451
D 2709	HEF4052BP	5322 209 14233
D 2711	OQ 0012	5322 209 85484
D 2901	TL082CP	5322 209 86064
D 2902	NE521N	5322 209 14441
D 2903	N74LS132N	5322 209 85201
D 2904	GXB10231P	5322 209 86003
D 2906	GXB10125P	5322 209 86119
D 2907	GXB10116P	5322 209 86441
D 2908	SN74LS151N-00	5322 209 86452
D 2909	SN74S74N-00	5322 209 84183
D 2911	N74LS04N	5322 209 85486
D 2912	N74S00N	5322 209 84167
D 3001	EN H GATE	5322 209 86491
D 3002	UA741CN	4822 209 80617

POSNR	DESCRIPTION	ORDERING CODE
D 3003	TL082CP	5322 209 86064
D 3004	SL3145E	5322 130 34554
D 3006	TL082CP	5322 209 86064
D 3101	BG2000-641/001	5322 218 61001

POSNR	DESCRIPTION			ORDERING CODE
R 4	47K	20	0.1W	5322 101 64031
R 401	6,19K	1	MR25	5322 116 50608
R 402	6,19K	1	MR25	5322 116 50608
R 403	15,4K	1	MR25	5322 116 50479
R 404	30,1K	1	MR25	5322 116 54655
R 406	6,19K	1	MR25	5322 116 50608
R 407	6,19K	1	MR25	5322 116 50608
R 408	105K	1	MR25	5322 116 54698
R 409	6,19K	1	MR25	5322 116 50608
R 411	6,19K	1	MR25	5322 116 50608
R 412	6,19K	1	MR25	5322 116 50608
R 413	301K	1	MR25	5322 116 54743
R 414	15,4K	1	MR25	5322 116 50479
R 416	6,19K	1	MR25	5322 116 50608
R 417	6,19K	1	MR25	5322 116 50608
R 418	105K	1	MR25	5322 116 54698
R 419	6,19K	1	MR25	5322 116 50608
R 421	301K	1	MR25	5322 116 54743
R 422	2,26K	1	MR25	5322 116 50675
R 423	2,26K	1	MR25	5322 116 50675
R 5	47K	20	0.1W	5322 101 64031
R 6	47K	20	0.1W	5322 101 64031
R 601	2,26K	1	MR25	5322 116 50675
R 602	2,26K	1	MR25	5322 116 50675
R 603	121	1	MR25	5322 116 54426
R 604	121	1	MR25	5322 116 54426
R 606	5,11	1	MR25	5322 116 54192
R 607	5,11	1	MR25	5322 116 54192
R 608	4,02K	1	MR25	5322 116 55448
R 609	4,02K	1	MR25	5322 116 55448
R 7	4,7K	20	0.1W	5322 101 40098
R 701	105	1	MR25	5322 116 54472
R 702	4,02K	1	MR25	5322 116 55448
R 8	4,7K	20	0.1W	5322 101 40098
R 801	3,3K	2	9X0.2W	5322 111 94255
R 9	47K	20	0.1W	5322 101 64032
R 901	2,26K	1	MR25	5322 116 50675
R 902	105	1	MR25	5322 116 54472
R 903	2,26K	1	MR25	5322 116 50675
R 904	2,26K	1	MR25	5322 116 50675
R 905	4,02K	1	MR25	5322 116 55448
R 906	2,26K	1	MR25	5322 116 50675
R 907	2,26K	1	MR25	5322 116 50675
R 908	2,26K	1	MR25	5322 116 50675
R 909	2,26K	1	MR25	5322 116 50675
R 911	2,26K	1	MR25	5322 116 50675
R 912	2,26K	1	MR25	5322 116 50675
R 1	47K	20	0.1W	5322 101 24185
R 10	10K	20	0.1W	5322 102 40059
R 1001	2,05K	1	MR25	5322 116 50664
R 1002	2,2K	20	0.5W	5322 100 10117

POSNR	DESCRIPTION			ORDERING CODE
R 1003	51,1	1	MR25	5322 116 54442
R 1004	51,1	1	MR25	5322 116 54442
R 1006	4,7K	20	0.5W	5322 101 14292
R 1007	10K	20	0.5W	5322 101 14066
R 1008	1K	20	0.5W	5322 101 10294
R 1009	2,05K	1	MR25	5322 116 50664
R 101	499	1	MR25	5322 116 54524
R 1011	6,19K	1	MR25	5322 116 50608
R 1012	6,19K	1	MR25	5322 116 50608
R 1013	51,1	1	MR25	5322 116 54442
R 1014	51,1	1	MR25	5322 116 54442
R 1016	4,64K	1	MR25	5322 116 50484
R 1017	2,61K	1	MR25	5322 116 50671
R 1018	6,19K	1	MR25	5322 116 50608
R 1019	1,21K	1	MR25	5322 116 54557
R 1021	649	1	MR25	5322 116 54532
R 1022	215	1	MR25	5322 116 55274
R 1023	10	1	MR25	5322 116 50452
R 1024	4,7K	20	0.5W	5322 101 14292
R 1026	10K	20	0.5W	5322 101 14066
R 1027	4,7K	20	0.5W	5322 101 14292
R 1028	3,48K	1	MR25	5322 116 54585
R 1029	5,36K	1	MR25	5322 116 54597
R 1031	4,42K	1	MR25	5322 116 50556
R 1032	1K	1	MR25	5322 116 54549
R 1033	1K	1	MR25	5322 116 54549
R 1034	100	1	MR25	5322 116 54469
R 1036	1K	1	MR25	5322 116 54549
R 1037	4,87K	1	MR25	5322 116 50509
R 1038	78,7	1	MR25	5322 116 50578
R 1039	127	1	MR25	5322 116 54479
R 1041	1K	1	MR25	5322 116 54549
R 1042	511	1	MR25	4822 116 51282
R 1043	511	1	MR25	4822 116 51282
R 1044	511	1	MR25	4822 116 51282
R 1046	511	1	MR25	4822 116 51282
R 1047	1K	1	MR25	5322 116 54549
R 1048	1K	1	MR25	5322 116 54549
R 1049	1K	1	MR25	5322 116 54549
R 1051	1K	1	MR25	5322 116 54549
R 1052	1K	1	MR25	5322 116 54549
R 1053	511	1	MR25	4822 116 51282
R 1054	511	1	MR25	4822 116 51282
R 1055	511	1	MR25	4822 116 51282
R 1056	1K	1	MR25	5322 116 54549
R 1057	4,02K	1	MR25	5322 116 55448
R 1058	100	1	MR25	5322 116 54469
R 1059	2,15K	1	MR25	5322 116 50767
R 1061	2,37K	1	MR25	5322 116 54576
R 1062	2,74K	1	MR25	5322 116 50636
R 1063	15,4K	1	MR25	5322 116 50479
R 1064	5,11K	1	MR25	5322 116 54595
R 1066	8,66K	1	MR25	5322 116 54613
R 1067	2,74K	1	MR25	5322 116 50636
R 1068	10K	1	MR25	4822 116 51253
R 1069	15,4K	1	MR25	5322 116 50479
R 1071	2,37K	1	MR25	5322 116 54576
R 1072	1K	1	MR25	5322 116 54549
R 1073	511	1	MR25	4822 116 51282
R 1074	1K	1	MR25	5322 116 54549
R 1075	100	1	MR25	5322 116 54469
R 1076	511	1	MR25	4822 116 51282
R 1077	4,64K	1	MR25	5322 116 50484
R 1078	40,2K	1	MR25	5322 116 54665
R 1079	1K	1	MR25	5322 116 54549

POSNR	DESCRIPTION			ORDERING CODE
R 1080	1K	20	0.5W	5322 101 10294
R 1081	1K	1	MR25	5322 116 54549
R 1082	2,37K	1	MR25	5322 116 54576
R 1083	2,37K	1	MR25	5322 116 54576
R 1084	1K	1	MR25	5322 116 54549
R 1086	1K	1	MR25	5322 116 54549
R 1087	2,05K	1	MR25	5322 116 50664
R 1088	6,19K	1	MR25	5322 116 50608
R 1089	4,87K	1	MR25	5322 116 50509
R 1090	5,62K	1	MR25	4822 116 51281
R 1091	1K	1	MR25	5322 116 54549
R 1092	4,64K	1	MR25	5322 116 50484
R 1093	40,2K	1	MR25	5322 116 54665
R 1094	5,11K	1	MR25	5322 116 54595
R 1096	5,9K	1	MR25	5322 116 50583
R 1097	59	1	MR25	5322 116 54448
R 1098	5,11K	1	MR25	5322 116 54595
R 1099	5,11K	1	MR25	5322 116 54595
R 1101	2,2K	20	0.5W	5322 101 10319
R 1102	2,2K	20	0.5W	5322 101 10319
R 1103	40,2K	1	MR25	5322 116 54665
R 1104	2,05K	1	MR25	5322 116 50664
R 1106	511	1	MR25	4822 116 51282
R 1107	1K	1	MR25	5322 116 54549
R 1108	1K	1	MR25	5322 116 54549
R 1109	1K	1	MR25	5322 116 54549
R 1111	365	1	MR25	5322 116 54516
R 1112	2,26K	1	MR25	5322 116 50675
R 1113	2,05K	1	MR25	5322 116 50664
R 1114	10K	1	MR25	4822 116 51253
R 1116	1,1K	1	MR25	4822 116 51236
R 1117	825	1	MR25	5322 116 54541
R 1118	44,2	1	MR25	5322 116 50818
R 1119	8,25K	1	MR25	5322 116 54558
R 1121	3,48K	1	MR25	5322 116 54585
R 1122	3,48K	1	MR25	5322 116 54585
R 1123	100	1	MR25	5322 116 54469
R 1124	22,6K	1	MR25	5322 116 50481
R 1126	22,6K	1	MR25	5322 116 50481
R 1127	4,42K	1	MR25	5322 116 50556
R 1128	10K	1	MR25	4822 116 51253
R 1129	1,1K	1	MR25	4822 116 51236
R 1130	6,8K	10	0.5W	5322 116 34058
R 1131	825	1	MR25	5322 116 54541
R 1132	2,26K	1	MR25	5322 116 50675
R 1133	365	1	MR25	5322 116 54516
R 1134	1,1K	1	MR25	4822 116 51236
R 1136	1,1K	1	MR25	4822 116 51236
R 1137	100	1	MR25	5322 116 54469
R 1138	40,2K	1	MR25	5322 116 54665
R 1139	2,05K	1	MR25	5322 116 50664
R 1141	44,2	1	MR25	5322 116 50818
R 12	10K	20	0.1W	5322 102 40058
R 1201	10K	1	MR25	4822 116 51253
R 1202	100K	1	MR25	4822 116 51268
R 1203	100K	1	MR25	4822 116 51268
R 1204	332K	1	MR25	4822 116 51184
R 1206	22,6K	1	MR25	5322 116 50481
R 1208	511	1	MR25	4822 116 51282
R 1209	2,26K	1	MR25	5322 116 50675
R 1211	2,26K	1	MR25	5322 116 50675
R 1212	2,26K	1	MR25	5322 116 50675
R 1213	2,26K	1	MR25	5322 116 50675
R 1214	2,26K	1	MR25	5322 116 50675
R 1216	511	1	MR25	4822 116 51282

POSNR	DESCRIPTION			ORDERING CODE
R 1217	511	1	MR25	4822 116 51282
R 1218	2,26K	1	MR25	5322 116 50675
R 1219	2,26K	1	MR25	5322 116 50675
R 1221	2,26K	1	MR25	5322 116 50675
R 1222	2,26K	1	MR25	5322 116 50675
R 1223	2,26K	1	MR25	5322 116 50675
R 1224	2,26K	1	MR25	5322 116 50675
R 1225	4,87K	1	MR25	5322 116 50509
R 1226	2,26K	1	MR25	5322 116 50675
R 1227	2,26K	1	MR25	5322 116 50675
R 1228	2,26K	1	MR25	5322 116 50675
R 1229	681	1	MR25	4822 116 51233
R 1230	3,01K	1	MR25	4822 116 51246
R 1301	133	1	MR25	5322 116 54482
R 1302	82,5	1	MR25	5322 116 54462
R 1303	205	1	MR25	5322 116 50669
R 1304	205	1	MR25	5322 116 50669
R 1306	205	1	MR25	5322 116 50669
R 1307	1K	1	MR25	5322 116 54549
R 1308	1K	1	MR25	5322 116 54549
R 1309	1K	1	MR25	5322 116 54549
R 1311	5,11K	1	MR25	5322 116 54595
R 1312	2,26K	1	MR25	5322 116 50675
R 1313	2,26K	1	MR25	5322 116 50675
R 1314	2,26K	1	MR25	5322 116 50675
R 1316	2,26K	1	MR25	5322 116 50675
R 1317	2,26K	1	MR25	5322 116 50675
R 1318	2,26K	1	MR25	5322 116 50675
R 1319	2,26K	1	MR25	5322 116 50675
R 1321	2,26K	1	MR25	5322 116 50675
R 1322	1K	1	MR25	5322 116 54549
R 1323	1K	1	MR25	5322 116 54549
R 1324	2,26K	1	MR25	5322 116 50675
R 1326	2,26K	1	MR25	5322 116 50675
R 1327	10	1	MR25	5322 116 50452
R 1328	10	1	MR25	5322 116 50452
R 1329	10K	1	MR25	4822 116 51253
R 1331	30,1K	1	MR25	5322 116 54655
R 1332	10K	1	MR25	4822 116 51253
R 1333	4,02K	1	MR25	5322 116 55448
R 1334	2,74K	1	MR25	5322 116 50636
R 1336	681	1	MR25	4822 116 51233
R 1337	1K	1	MR25	5322 116 54549
R 1338	4,02K	1	MR25	5322 116 55448
R 14	100K	20		5322 101 44037
R 15	47K	20	0.1W	5322 101 24203
R 1501	31,6K	1	MR25	5322 116 54657
R 1502	6,8M	5	VR37	4822 110 42209
R 1503	402	1	MR25	5322 116 54519
R 1504	31,6M	1	VR37	5322 116 64103
R 1506	1M	20	0.5W	5322 101 14068
R 1507				4822 116 40031
R 1508	10K	1	MR25	4822 116 51253
R 1509	2,2M	5	VR37	4822 110 42196
R 1511	4,64K	1	MR25	5322 116 50484
R 1512	7,5	1	MR25	5322 116 54417
R 1513	7,5	1	MR25	5322 116 54417
R 1514	10K	1	MR25	4822 116 51253
R 1516	402K	1	MR25	5322 116 55283
R 1517	1M	1	MR25	5322 116 55535
R 1518	402K	1	MR25	5322 116 55283
R 1519	1M	1	MR25	5322 116 55535
R 1521	511	1	MR25	4822 116 51282
R 1522	10M	1	VR37	4822 110 42214
R 1523	226	1	MR25	5322 116 54497

POSNR	DESCRIPTION			ORDERING CODE
R 1524	226	1	MR25	5322 116 54497
R 1526	5,11K	1	MR25	5322 116 54595
R 1527	5,11	1	MR25	5322 116 54192
R 1528	5,11	1	MR25	5322 116 54192
R 1529	5,11	1	MR25	5322 116 54192
R 1531	1M	1	MR25	5322 116 55535
R 1532	1,33K	1	MR25	5322 116 54561
R 1533	1,33K	1	MR25	5322 116 54561
R 1534	1K	1	MR25	5322 116 54549
R 1536	511K	1	MR25	5322 116 55258
R 1537	68,1K	1	MR25	5322 116 54683
R 1538	68,1K	1	MR25	5322 116 54683
R 1539	22,6K	1	MR25	5322 116 50481
R 1541	681K	1	MR25	5322 116 55284
R 1542	100	1	MR25	5322 116 54469
R 1543	100	1	MR25	5322 116 54469
R 1544	5,11K	1	MR25	5322 116 54595
R 1546	121	1	MR25	5322 116 54426
R 1547	82,5	1	MR25	5322 116 54462
R 1548	825	1	MR25	5322 116 54541
R 1549	1K	1	MR25	5322 116 54549
R 1551	249K	1	MR25	5322 116 54386
R 1552	3,48K	1	MR25	5322 116 54585
R 1553	68,1K	1	MR25	5322 116 54683
R 1554	40,2K	1	MR25	5322 116 54665
R 1556	274	1	MR25	5322 116 54504
R 1557	21,5K	1	MR25	5322 116 50451
R 1558	15,4K	1	MR25	5322 116 50479
R 1559	1,33K	1	MR25	5322 116 54561
R 1561	825	1	MR25	5322 116 54541
R 1562	274	1	MR25	5322 116 54504
R 1563	36,5K	1	MR25	5322 116 50726
R 1564	6,81K	1	MR25	4822 116 51252
R 1566	22,6K	1	MR25	5322 116 50481
R 1567	22,6K	1	MR25	5322 116 50481
R 1568	3,01K	1	MR25	4822 116 51246
R 1569	30,1K	1	MR25	5322 116 54655
R 1571	26,1K	1	MR25	5322 116 54651
R 1572	6,81K	1	MR25	4822 116 51252
R 1573	11K	1	MR25	5322 116 54623
R 1574	3,01K	1	MR25	4822 116 51246
R 1576	10K	1	MR25	4822 116 51253
R 1577	8,25K	1	MR25	5322 116 54558
R 1578	7,87K	1	MR25	5322 116 50458
R 1579	1M	1	MR25	5322 116 55535
R 1581	10K	1	MR25	4822 116 51253
R 1582	3,01K	1	MR25	4822 116 51246
R 1583	3,01K	1	MR25	4822 116 51246
R 1584	3,01K	1	MR25	4822 116 51246
R 1586	18,7K	1	MR25	5322 116 50558
R 1587	47K	20	0.5W	5322 101 14293
R 1588	2,2K	20	0.5W	5322 100 10117
R 1589	2,2K	20	0.5W	5322 100 10117
R 1591	1K	20	0.5W	5322 101 10294
R 1592	18,7K	1	MR25	5322 116 50558
R 16	4,7K	20	0.1W	5322 101 24186
R 1601	301K	1	MR25	5322 116 54743
R 1602	301K	1	MR25	5322 116 54743
R 1603	2K	5	PR52	5322 116 55205
R 1604	20	5	PR52	5322 116 54351
R 1605	22,6	1	MR25	5322 116 50491
R 1606	110K	0,5	MR30	5322 116 55485
R 1607	20,5K	1	MR25	5322 116 54643
R 1608	100K	1	MR25	4822 116 51268
R 1609	40,2K	1	MR25	5322 116 54665

POSNR	DESCRIPTION			ORDERING CODE
R 1611	22,6K	1	MR25	5322 116 50481
R 1612	33,2K	1	MR25	4822 116 51259
R 1613	1M	5	VR37	4822 110 42187
R 1614	215K	0,5	MR30	5322 116 55529
R 1616	3,3K	5	4W	4822 112 21121
R 1617	1M	5	VR37	4822 110 42187
R 1618	215K	0,5	MR30	5322 116 55529
R 1619	27K	5	PR52	5322 116 54983
R 1620	1,54K	1	MR25	5322 116 50586
R 1621	27K	5	PR52	5322 116 54983
R 1622	110K	0,5	MR30	5322 116 55485
R 1623	24,9K	1	MR25	5322 116 54648
R 1624	6,81K	1	MR25	4822 116 51252
R 1626	249	1	MR25	5322 116 54499
R 1627	1	1	MR25	4822 116 51179
R 1628	100	1	MR25	5322 116 54469
R 1629	10	1	MR25	5322 116 50452
R 1631	1K5	25%		5322 116 34051
R 1632	12,1K	1	MR25	5322 116 50572
R 1633	825	1	MR25	5322 116 54541
R 1634	140	1	MR25	5322 116 54484
R 1636	249	1	MR25	5322 116 54499
R 1637	3,32K	1	MR25	5322 116 54005
R 1638	2,26K	1	MR25	5322 116 50675
R 1639	4,87K	1	MR25	5322 116 50509
R 1641	4,64K	1	MR25	5322 116 50484
R 1642	16,2K	1	MR25	5322 116 55361
R 1643	100K	1	MR25	4822 116 51268
R 1644	5,11	1	MR25	5322 116 54192
R 1646	470	20	0.5W	5322 101 14049
R 1647	4,7K	20	0.5W	5322 101 14292
R 1648	4,42K	1	MR25	5322 116 50556
R 2	10K	20	0.1W	5322 101 44049
R 2001	681K	1	MR25	5322 116 55284
R 2002	681K	1	MR25	5322 116 55284
R 2003	681K	1	MR25	5322 116 55284
R 2004	681K	1	MR25	5322 116 55284
R 2006	681K	1	MR25	5322 116 55284
R 2007	681K	1	MR25	5322 116 55284
R 2008	2,2K	20	0.5W	5322 100 10117
R 2009	4,7K	20	0.5W	5322 101 14292
R 201	237	1	MR25	5322 116 50679
R 2011	47K	20	0.5W	5322 101 14293
R 2012	3,16K	1	MR25	5322 116 50579
R 2013	16,9K	1	MR25	5322 116 54635
R 2014	10K	1	MR25	4822 116 51253
R 2016	511	1	MR25	4822 116 51282
R 2017	1K	20	0.5W	5322 101 10294
R 2018	4,7K	20	0.5W	5322 101 14292
R 2019	22K	20	0.5W	5322 100 10118
R 202	237	1	MR25	5322 116 50679
R 2021	20,5K	1	MR25	5322 116 54643
R 2022	10K	1	MR25	4822 116 51253
R 2023	19,6K	1	MR25	5322 116 54641
R 2024	10K	1	MR25	4822 116 51253
R 2026	3,32K	1	MR25	5322 116 54005
R 2027	178	1	MR25	5322 116 54492
R 2028	10K	1	MR25	4822 116 51253
R 2029	10K	1	MR25	4822 116 51253
R 203	237	1	MR25	5322 116 50679
R 2031	23,7K	1	MR25	5322 116 54646
R 2032	10K	1	MR25	4822 116 51253
R 2033	10K	1	MR25	4822 116 51253
R 2034	10K	1	MR25	4822 116 51253
R 2036	100K	1	MR25	4822 116 51268

POSNR	DESCRIPTION			ORDERING CODE
R 2037	5,36K	1	MR25	5322 116 54597
R 2038	1K	1	MR25	5322 116 54549
R 2039	4,7K	20	0.5W	5322 101 14292
R 204	237	1	MR25	5322 116 50679
R 2041	5,36K	1	MR25	5322 116 54597
R 2042	10K	1	MR25	4822 116 51253
R 2043	1,87K	1	MR25	5322 116 50728
R 2044	22,6K	1	MR25	5322 116 50481
R 2046	2,05K	1	MR25	5322 116 50664
R 2047	100	1	MR25	5322 116 54469
R 2048	24,9K	1	MR25	5322 116 54648
R 2049	154K	1	MR25	5322 116 54714
R 2051	154K	1	MR25	5322 116 54714
R 2052	1K	1	MR25	5322 116 54549
R 2053	10K	1	MR25	4822 116 51253
R 2054	10K	1	MR25	4822 116 51253
R 2056	10K	1	MR25	4822 116 51253
R 2057	51,1K	1	MR25	5322 116 50672
R 2058	51,1K	1	MR25	5322 116 50672
R 2059	10K	1	MR25	4822 116 51253
R 206	237	1	MR25	5322 116 50679
R 2061	10K	1	MR25	4822 116 51253
R 2062	10K	1	MR25	4822 116 51253
R 2063	154K	1	MR25	5322 116 54714
R 2064	511K	1	MR25	5322 116 55258
R 2066	7,15K	1	MR25	5322 116 54606
R 2067	7,15K	1	MR25	5322 116 54606
R 2068	100K	1	MR25	4822 116 51268
R 2069	3,83K	1	MR25	5322 116 54589
R 207	237	1	MR25	5322 116 50679
R 2071	169K	1	MR25	5322 116 54718
R 2072	100K	20	0.5W	5322 100 10116
R 2073	10K	1	MR25	4822 116 51253
R 2074	7,15K	1	MR25	5322 116 54606
R 2076	3,83K	1	MR25	5322 116 54589
R 2077	10K	1	MR25	4822 116 51253
R 2078	7,15K	1	MR25	5322 116 54606
R 2079	1,96K	1	MR25	5322 116 54571
R 208	237	1	MR25	5322 116 50679
R 2080	3,83K	1	MR25	5322 116 54589
R 2081	1,96K	1	MR25	5322 116 54571
R 2082	6,19K	1	MR25	5322 116 50608
R 2083	301K	1	MR25	5322 116 54743
R 2084	24,9K	1	MR25	5322 116 54648
R 2085	3,83K	1	MR25	5322 116 54589
R 2086	100K	1	MR25	4822 116 51268
R 2087	5,36K	1	MR25	5322 116 54597
R 2088	154K	1	MR25	5322 116 54714
R 2089	10K	1	MR25	4822 116 51253
R 209	237	1	MR25	5322 116 50679
R 2091	5,36K	1	MR25	5322 116 54597
R 2092	154K	1	MR25	5322 116 54714
R 2093	1,78K	1	MR25	5322 116 50515
R 2094	3,01K	1	MR25	4822 116 51246
R 2096	10K	1	MR25	4822 116 51253
R 2097	154K	1	MR25	5322 116 54714
R 2098	2,37K	1	MR25	5322 116 54576
R 2099	15,4K	1	MR25	5322 116 50479
R 2101	30,1K	1	MR25	5322 116 54655
R 2102	953	1	MR25	5322 116 54547
R 2103	2,37K	1	MR25	5322 116 54576
R 2104	5,11	1	MR25	5322 116 54192
R 2106	5,11	1	MR25	5322 116 54192
R 2107	16,2K	1	MR25	5322 116 55361
R 2108	5,11	1	MR25	5322 116 54192

POSNR	DESCRIPTION			ORDERING CODE
R 2109	487	1	MR25	5322 116 55451
R 211	237	1	MR25	5322 116 50679
R 2111	2,74K	1	MR25	5322 116 50636
R 2112	10,5K	1	MR25	5322 116 50731
R 2113	5,11	1	MR25	5322 116 54192
R 2114	5,11	1	MR25	5322 116 54192
R 2116	5,11K	1	MR25	5322 116 54595
R 2118	75K	1	MR25	5322 116 54686
R 2119	5,11	1	MR25	5322 116 54192
R 212	237	1	MR25	5322 116 50679
R 2121	10K	1	MR25	4822 116 51253
R 2122	3,01K	1	MR25	4822 116 51246
R 2123	20,5K	1	MR25	5322 116 54643
R 2124	10K	1	MR25	4822 116 51253
R 2126	5,11	1	MR25	5322 116 54192
R 213	237	1	MR25	5322 116 50679
R 214	1,15K	1	MR25	5322 116 50415
R 216	1,15K	1	MR25	5322 116 50415
R 217	1,15K	1	MR25	5322 116 50415
R 218	1,15K	1	MR25	5322 116 50415
R 219	1,15K	1	MR25	5322 116 50415
R 221	1,15K	1	MR25	5322 116 50415
R 222	237	1	MR25	5322 116 50679
R 223	237	1	MR25	5322 116 50679
R 231	20,5K	1	MR25	5322 116 54643
R 232	20,5K	1	MR25	5322 116 54643
R 2400	5,6M	5	VR25	4822 110 72207
R 2401	100K	1	MR25	4822 116 51268
R 2402	100K	1	MR25	4822 116 51268
R 2403	100K	1	MR25	4822 116 51268
R 2404	100K	1	MR25	4822 116 51268
R 2406	33,2K	1	MR25	4822 116 51259
R 2407	10,5K	1	MR25	5322 116 50731
R 2408	7,5K	1	MR25	5322 116 54608
R 2409	2,15K	1	MR25	5322 116 50767
R 241	6,81K	1	MR25	4822 116 51252
R 2410	1,5M	5	VR25	4822 110 72192
R 2411	2,2K	20	0.5W	5322 101 14008
R 2412	2,05K	1	MR25	5322 116 50664
R 2413	992K	0,5	SPEC	5322 116 55153
R 2414	51,1	1	MR25	5322 116 54442
R 2415	3,3M	5	VR25	4822 110 72201
R 2416	22K	20	0.5W	5322 101 14069
R 2417	2,87K	1	MR25	5322 116 50414
R 2418	100	1	MR25	5322 116 54469
R 2419	1K	1	MR25	5322 116 54549
R 242	6,81K	1	MR25	4822 116 51252
R 2420	14	1	MR25	5322 116 50839
R 2421	64,9K	1	MR25	5322 116 50514
R 2422	560	5	CR16	4822 111 30309
R 2423	10	5	CR16	4822 111 30347
R 2424	1K	1	MR25	5322 116 54549
R 2425	1,54K	1	MR25	5322 116 50586
R 2426	100M	5	0,125W	5322 111 30376
R 2428	287	1	MR25	5322 116 54506
R 2429	287	1	MR25	5322 116 54506
R 243	6,81K	1	MR25	4822 116 51252
R 2431	5,36K	1	MR25	5322 116 54597
R 2432	71,5K	1	MR25	5322 116 54685
R 2433	20,5K	1	MR25	5322 116 54643
R 2434	64,9K	1	MR25	5322 116 50514
R 2436	33	5	CR16	4822 111 30067
R 2437	64,9	1	MR25	5322 116 54453
R 2438	115	1	MR25	5322 116 54476
R 2439	124	1	MR25	5322 116 54478

POSNR	DESCRIPTION			ORDERING CODE
R 244	6,81K	1	MR25	4822 116 51252
R 2441	261	1	MR25	5322 116 54502
R 2442	10K	1	MR25	4822 116 51253
R 2443	7,15K	1	MR25	5322 116 54606
R 2444	5,11	1	MR25	5322 116 54192
R 2446	21,5K	1	MR25	5322 116 50451
R 2448	8,06K	0,5	MR25	5322 116 55428
R 2449	2,26K	1	MR25	5322 116 50675
R 2450	6,81	1	MR25	5322 116 54013
R 2451	48,7K	1	MR25	5322 116 50442
R 2452	105	1	MR25	5322 116 54472
R 2453	95,3	1	MR25	5322 116 50569
R 2454	1,58K	1	MR25	5322 116 50622
R 2455	51,1K	1	MR25	5322 116 50672
R 2456	95,3	1	MR25	5322 116 50569
R 2457	5,9K	1	MR25	5322 116 50583
R 2458	3,32K	1	MR25	5322 116 54005
R 2459	22	5	CR16	5322 111 30396
R 246	6,81K	1	MR25	4822 116 51252
R 2461	249K	1	MR25	5322 116 54386
R 2462	22,6	1	MR25	5322 116 50491
R 2463	27	5	CR16	4822 111 30348
R 2464	33	5	CR16	4822 111 30067
R 2466	806K	0,5	MR25	5322 116 51369
R 2467	226K	1	MR25	5322 116 54729
R 2468	82,5	1	MR25	5322 116 54462
R 2469	18,7	1	MR25	5322 116 50895
R 247	6,81K	1	MR25	4822 116 51252
R 2470	1K	1	MR16	5322 116 55393
R 2471	560	5	CR16	4822 111 30309
R 2472	15	5	CR16	5322 111 44153
R 2473	200K	0,5	MR30	5322 116 51371
R 2474	51,1	1	MR25	5322 116 54442
R 2475	1K	1	MR16	5322 116 55393
R 2476	42,2	1	MR25	5322 116 51052
R 2477	100K	1	MR25	4822 116 51268
R 2478	42,2	1	MR25	5322 116 51052
R 2479	920K	0,5	MR30	5322 116 55218
R 248	6,81K	1	MR25	4822 116 51252
R 2481	22K	20	0.5W	5322 101 14069
R 2482	86,6	1	MR25	5322 116 54464
R 2483	5,11	1	MR25	5322 116 54192
R 2484	18,7	1	MR25	5322 116 50895
R 2485	953K	1	MR25	5322 116 51368
R 2486	402K	1	MR25	5322 116 55283
R 2487	86,6	1	MR25	5322 116 54464
R 2488	5,11	1	MR25	5322 116 54192
R 2489	301	1	MR25	5322 116 54508
R 249	6,81K	1	MR25	4822 116 51252
R 2490	511	1	MR25	4822 116 51282
R 2491	301	1	MR25	5322 116 54508
R 2492	301	1	MR25	5322 116 54508
R 2493	806K	0,5	MR25	5322 116 51369
R 2494	53,6K	1	MR25	5322 116 54674
R 2496	205	1	MR25	5322 116 50669
R 2497	5,36K	1	MR25	5322 116 54597
R 2498	11K	1	MR25	5322 116 54623
R 2499	61,9	1	MR25	5322 116 54451
R 2501	402	1	MR25	5322 116 54519
R 2504	100	1	MR25	5322 116 54469
R 2506	100	1	MR25	5322 116 54469
R 2507	5,36K	1	MR25	5322 116 54597
R 2509	715	1	MR25	5322 116 50571
R 251	6,81K	1	MR25	4822 116 51252
R 2511	100K	1	MR25	4822 116 51268

POSNR	DESCRIPTION			ORDERING CODE
R 2512	590	1	MR25	5322 116 50561
R 2513	8,25K	1	MR25	5322 116 54558
R 2514	14,7K	1	MR25	5322 116 54632
R 2516	51,1	1	MR25	5322 116 54442
R 2517	100	1	MR25	5322 116 54469
R 2518	1K	1	MR25	5322 116 54549
R 2519	681	1	MR25	4822 116 51233
R 252	6,81K	1	MR25	4822 116 51252
R 2520	14	1	MR25	5322 116 50839
R 2521	88,7K	0,5	MR25	5322 116 55452
R 2522	7,15K	1	MR25	5322 116 54606
R 2523	100K	1	MR25	4822 116 51268
R 2524	10	1	MR25	5322 116 50452
R 2526	1K	20	0,5W	5322 100 10112
R 2527	1K	20	0,5W	5322 100 10112
R 2528	1,05K	1	MR25	5322 116 54552
R 2529	51,1	1	MR25	5322 116 54442
R 253	6,81K	1	MR25	4822 116 51252
R 2530	100	1	MR25	5322 116 54469
R 2531	15,4K	1	MR25	5322 116 50479
R 2532	1,69K	1	MR25	5322 116 54567
R 2533	1,05K	1	MR25	5322 116 54552
R 2534	10K	20	0,5W	5322 100 10113
R 2535	100	1	MR25	5322 116 54469
R 2536	1K	20	0,5W	5322 100 10112
R 2539	301	1	MR25	5322 116 54508
R 254	6,81K	1	MR25	4822 116 51252
R 2541	5,9K	1	MR25	5322 116 50583
R 2542	1,4K	1	MR25	5322 116 54562
R 2543	301	1	MR25	5322 116 54508
R 2544	560	5	CR16	4822 111 30309
R 2545	150	1	MR25	5322 116 54486
R 2546	992K	0,5	SPEC	5322 116 55153
R 2547	10	1	MR25	5322 116 50452
R 2548	51,1	1	MR25	5322 116 54442
R 2549	2,87K	1	MR25	5322 116 50414
R 2551	287	1	MR25	5322 116 54506
R 2552	287	1	MR25	5322 116 54506
R 2553	5,36K	1	MR25	5322 116 54597
R 2554	71,5K	1	MR25	5322 116 54685
R 2556	20,5K	1	MR25	5322 116 54643
R 2557	51,1	1	MR25	5322 116 54442
R 2558	1K	1	MR25	5322 116 54549
R 2559	10	5	CR16	4822 111 30347
R 256	6,81K	1	MR25	4822 116 51252
R 2560	1,54K	1	MR25	5322 116 50586
R 2561	1K	1	MR25	5322 116 54549
R 2562	100M	5	0,125W	5322 111 30376
R 2564	5,11	1	MR25	5322 116 54192
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R 2568	33	5	CR16	4822 111 30067
R 2569	64,9	1	MR25	5322 116 54453
R 257	6,81K	1	MR25	4822 116 51252
R 2571	115	1	MR25	5322 116 54476
R 2572	124	1	MR25	5322 116 54478
R 2573	261	1	MR25	5322 116 54502
R 2574	9,09K	1	MR25	4822 116 51284
R 2576	22K	20	0.5W	5322 101 14069
R 2577	100	1	MR25	5322 116 54469
R 2578	8,06K	0,5	MR25	5322 116 55428
R 2579	2,26K	1	MR25	5322 116 50675
R 258	6,81K	1	MR25	4822 116 51252
R 2580	6,81	1	MR25	5322 116 54013
R 2581	48,7K	1	MR25	5322 116 50442
R 2582	105	1	MR25	5322 116 54472

POSNR	DESCRIPTION			ORDERING CODE
R 2583	90,9	1	MR25	5322 116 54466
R 2584	5,9K	1	MR25	5322 116 50583
R 2585	51,1K	1	MR25	5322 116 50672
R 2586	22	5	CR16	5322 111 30396
R 2587	249K	1	MR25	5322 116 54386
R 2588	90,9	1	MR25	5322 116 54466
R 2589	22,6	1	MR25	5322 116 50491
R 259	6,81K	1	MR25	4822 116 51252
R 2591	27	5	CR16	4822 111 30348
R 2592	33	5	CR16	4822 111 30067
R 2593	806K	0,5	MR25	5322 116 51369
R 2594	226K	1	MR25	5322 116 54729
R 2596	82,5	1	MR25	5322 116 54462
R 2597	18,7	1	MR25	5322 116 50895
R 2598	560	5	CR16	4822 111 30309
R 2599	15	5	CR16	5322 111 44153
R 2600	1K	1	MR16	5322 116 55393
R 2601	200K	0,5	MR30	5322 116 51371
R 2602	51,1	1	MR25	5322 116 54442
R 2603	301	1	MR25	5322 116 54508
R 2604	42,2	1	MR25	5322 116 51052
R 2605	1K	1	MR16	5322 116 55393
R 2606	100K	1	MR25	4822 116 51268
R 2607	301	1	MR25	5322 116 54508
R 2608	42,2	1	MR25	5322 116 51052
R 2609	920K	0,5	MR30	5322 116 55218
R 261	6,81K	1	MR25	4822 116 51252
R 2611	22K	20	0.5W	5322 101 14069
R 2612	86,6	1	MR25	5322 116 54464
R 2613	5,11	1	MR25	5322 116 54192
R 2614	18,7	1	MR25	5322 116 50895
R 2615	953K	1	MR25	5322 116 51368
R 2616	402K	1	MR25	5322 116 55283
R 2617	86,6	1	MR25	5322 116 54464
R 2618	5,11	1	MR25	5322 116 54192
R 2619	806K	0,5	MR25	5322 116 51369
R 262	6,81K	1	MR25	4822 116 51252
R 2620	511	1	MR25	4822 116 51282
R 2621	53,6K	1	MR25	5322 116 54674
R 2622	205	1	MR25	5322 116 50669
R 2623	5,36K	1	MR25	5322 116 54597
R 2624	11K	1	MR25	5322 116 54623
R 2626	61,9	1	MR25	5322 116 54451
R 2627	402	1	MR25	5322 116 54519
R 2628	5,36K	1	MR25	5322 116 54597
R 2629	15,4K	1	MR25	5322 116 50479
R 263	6,81K	1	MR25	4822 116 51252
R 2631	681	1	MR25	4822 116 51233
R 2632	100K	1	MR25	4822 116 51268
R 2633	590	1	MR25	5322 116 50561
R 2634	8,25K	1	MR25	5322 116 54558
R 2636	14,7K	1	MR25	5322 116 54632
R 2637	100	1	MR25	5322 116 54469
R 2638	88,7K	0,5	MR25	5322 116 55452
R 2639	7,15K	1	MR25	5322 116 54606
R 264	6,81K	1	MR25	4822 116 51252
R 2641	100K	1	MR25	4822 116 51268
R 2642	1K	20	0,5W	5322 100 10112
R 2643	1K	20	0,5W	5322 100 10112
R 2644	1,05K	1	MR25	5322 116 54552
R 2646	51,1	1	MR25	5322 116 54442
R 2647	15,4K	1	MR25	5322 116 50479
R 2648	1,69K	1	MR25	5322 116 54567
R 2649	7,15K	1	MR25	5322 116 54606
R 2651	100K	1	MR25	4822 116 51268

POSNR	DESCRIPTION			ORDERING CODE
R 2652	1,87K	1	MR25	5322 116 50728
R 2653	33,2K	1	MR25	4822 116 51259
R 2654	1,05K	1	MR25	5322 116 54552
R 2656	30,1	1	MR25	5322 116 50904
R 2657	10K	20	0,5W	5322 100 10113
R 2658	1K	20	0,5W	5322 100 10112
R 266	6,81K	1	MR25	4822 116 51252
R 2661	22K	20	0.5W	5322 101 14069
R 2662	30,1	1	MR25	5322 116 50904
R 2663	33,2K	1	MR25	4822 116 51259
R 2664	226K	1	MR25	5322 116 54729
R 2665	1K	1	MR25	5322 116 54549
R 2666	226K	1	MR25	5322 116 54729
R 2667	226K	1	MR25	5322 116 54729
R 2668	226K	1	MR25	5322 116 54729
R 2669	226K	1	MR25	5322 116 54729
R 267	6,81K	1	MR25	4822 116 51252
R 2670	511	1	MR25	4822 116 51282
R 2671	6,81K	1	MR25	4822 116 51252
R 2672	6,81K	1	MR25	4822 116 51252
R 2673	6,81K	1	MR25	4822 116 51252
R 2674	6,81K	1	MR25	4822 116 51252
R 2675	1,62K	1	MR25	5322 116 55359
R 2676	7,5K	1	MR25	5322 116 54608
R 2677	7,5K	1	MR25	5322 116 54608
R 2678	3,83K	1	MR25	5322 116 54589
R 2679	121	1	MR25	5322 116 54426
R 268	6,81K	1	MR25	4822 116 51252
R 2680	1,62K	1	MR25	5322 116 55359
R 2681	1,15K	1	MR25	5322 116 50415
R 2682	10K	1	MR25	4822 116 51253
R 2683	10K	1	MR25	4822 116 51253
R 2684	226K	1	MR25	5322 116 54729
R 2686	10K	1	MR25	4822 116 51253
R 2687	10K	1	MR25	4822 116 51253
R 2688	1K	1	MR25	5322 116 54549
R 269	6,81K	1	MR25	4822 116 51252
R 2690	1K	1	MR25	5322 116 54549
R 2701	909K	1	MR25	5322 116 55533
R 2702	110K	1	MR25	5322 116 54701
R 2703	681K	1	MR25	5322 116 55284
R 2704	100M	5	0,125W	5322 111 30376
R 2706	866	1	MR25	5322 116 54543
R 2707	7,87K	1	MR25	5322 116 50458
R 2708	5,11K	1	MR25	5322 116 54595
R 2709	5,11	1	MR25	5322 116 54192
R 271	2,26K	1	MR25	5322 116 50675
R 2711	10	1	MR25	5322 116 50452
R 2712	154K	1	MR25	5322 116 54714
R 2713	215K	1	MR25	5322 116 54728
R 2714	100	1	MR25	5322 116 54469
R 2716	10K	1	MR25	4822 116 51253
R 2717	10K	1	MR25	4822 116 51253
R 2718	5,11	1	MR25	5322 116 54192
R 2719	10	1	MR25	5322 116 50452
R 272	6,81K	1	MR25	4822 116 51252
R 2721	6,81K	1	MR25	4822 116 51252
R 2722	4,22K	1	MR25	5322 116 50729
R 2723	1,4K	1	MR25	5322 116 54562
R 2724	10K	1	MR25	4822 116 51253
R 2726	10K	1	MR25	4822 116 51253
R 2727	1K	1	MR25	5322 116 54549
R 2728	10K	1	MR25	4822 116 51253
R 2729	110K	1	MR25	5322 116 54701
R 273	2,26K	1	MR25	5322 116 50675

POSNR	DESCRIPTION			ORDERING CODE
R 2731	40,2K	1	MR25	5322 116 54665
R 2732	10K	1	MR25	4822 116 51253
R 2733	237K	1	MR25	5322 116 54732
R 2734	187K	1	MR25	5322 116 54723
R 2736	2,49K	1	MR25	5322 116 50581
R 2737	1,69K	1	MR25	5322 116 54567
R 2738	22,6	1	MR25	5322 116 50491
R 2739	205	1	MR25	5322 116 50669
R 274	6,81K	1	MR25	4822 116 51252
R 2741	681K	1	MR25	5322 116 55284
R 2742	6,81K	1	MR25	4822 116 51252
R 2743	10K	1	MR25	4822 116 51253
R 2744	10K	1	MR25	4822 116 51253
R 2746	10K	1	MR25	4822 116 51253
R 2747	51,1	1	MR25	5322 116 54442
R 2748	590	1	MR25	5322 116 50561
R 2749	10K	1	MR25	4822 116 51253
R 2751	715	1	MR25	5322 116 50571
R 2752	82,5K	1	MR25	5322 116 54689
R 2753	220	20	0,5W	5322 101 14009
R 2754	2,37K	1	MR25	5322 116 54576
R 2756	3,48K	1	MR25	5322 116 54585
R 2757	82,5K	1	MR25	5322 116 54689
R 2758	215K	1	MR25	5322 116 54728
R 2759	442	1	MR25	5322 116 50592
R 276	2,26K	1	MR25	5322 116 50675
R 2761	75K	1	MR25	5322 116 54686
R 2763	205	1	MR25	5322 116 50669
R 2764	681K	1	MR25	5322 116 55284
R 2766	6,81K	1	MR25	4822 116 51252
R 2767	100K	1	MR25	4822 116 51268
R 2768	1K	1	MR25	5322 116 54549
R 2769	590	1	MR25	5322 116 50561
R 277	6,81K	1	MR25	4822 116 51252
R 2771	10K	1	MR25	4822 116 51253
R 2772	6,81K	1	MR25	4822 116 51252
R 2773	22,6	1	MR25	5322 116 50491
R 2774	100	1	MR25	5322 116 54469
R 2776	2,74K	1	MR25	5322 116 50636
R 2777	3,83K	1	MR25	5322 116 54589
R 2778	140	1	MR25	5322 116 54484
R 2779	5,11	1	MR25	5322 116 54192
R 278	2,26K	1	MR25	5322 116 50675
R 2781	10,5K	1	MR25	5322 116 50731
R 2782	5,11	1	MR25	5322 116 54192
R 2783	100K	1	MR25	4822 116 51268
R 2784	100	1	MR25	5322 116 54469
R 2786	10K	1	MR25	4822 116 51253
R 2787	1K	1	MR25	5322 116 54549
R 2788	30,1K	1	MR25	5322 116 54655
R 2789	10K	1	MR25	4822 116 51253
R 279	6,81K	1	MR25	4822 116 51252
R 2791	30,1K	1	MR25	5322 116 54655
R 2792	10K	1	MR25	4822 116 51253
R 2793	3,32K	1	MR25	5322 116 54005
R 2794	78,7	1	MR25	5322 116 50578
R 2795	154	1	MR25	5322 116 50506
R 2796	1K	1	MR25	5322 116 54549
R 2797	3,32K	1	MR25	5322 116 54005
R 2798	3,01K	1	MR25	4822 116 51246
R 2799	1,54K	1	MR25	5322 116 50586
R 2801	10K	1	MR25	4822 116 51253
R 2802	10K	1	MR25	4822 116 51253
R 2803	10K	1	MR25	4822 116 51253
R 2804	10K	1	MR25	4822 116 51253

POSNR	DESCRIPTION			ORDERING CODE
R 2806	10K	1	MR25	4822 116 51253
R 2807	10K	1	MR25	4822 116 51253
R 2808	10K	1	MR25	4822 116 51253
R 2809	10K	1	MR25	4822 116 51253
R 281	2,26K	1	MR25	5322 116 50675
R 2811	115	1	MR25	5322 116 54476
R 2812	1K	1	MR25	5322 116 54549
R 2813	1K	1	MR25	5322 116 54549
R 2814	590	1	MR25	5322 116 50561
R 2816	10K	1	MR25	4822 116 51253
R 2817	115	1	MR25	5322 116 54476
R 2818	5,11K	1	MR25	5322 116 54595
R 2819	220	20	0,5W	5322 101 14009
R 282	6,81K	1	MR25	4822 116 51252
R 2820	787	1	MR25	5322 116 54538
R 2821	22,6	1	MR25	5322 116 50491
R 2822	383	1	MR25	5322 116 54518
R 2823	511	1	MR25	4822 116 51282
R 2824	1,54K	1	MR25	5322 116 50586
R 2825	51,1	1	MR25	5322 116 54442
R 2826	22,6	1	MR25	5322 116 50491
R 2827	2,49K	1	MR25	5322 116 50581
R 2828	1,27K	1	MR25	5322 116 50555
R 2829	590	1	MR25	5322 116 50561
R 283	2,26K	1	MR25	5322 116 50675
R 2830	51,1	1	MR25	5322 116 54442
R 2831	1,15K	1	MR25	5322 116 50415
R 2832	22,6	1	MR25	5322 116 50491
R 2833	511	1	MR25	4822 116 51282
R 2834	22,6	1	MR25	5322 116 50491
R 2835	348	1	MR25	5322 116 54515
R 2836	1,62K	1	MR25	5322 116 55359
R 2837	4,22K	1	MR25	5322 116 50729
R 2838	1,62K	1	MR25	5322 116 55359
R 2839	22,6	1	MR25	5322 116 50491
R 284	6,81K	1	MR25	4822 116 51252
R 2840	51,1	1	MR25	5322 116 54442
R 2841	22,6	1	MR25	5322 116 50491
R 2842	1,62K	1	MR25	5322 116 55359
R 2843	4,22K	1	MR25	5322 116 50729
R 2844	1,62K	1	MR25	5322 116 55359
R 2845	348	1	MR25	5322 116 54515
R 2846	22,6	1	MR25	5322 116 50491
R 2847	10K	1	MR25	4822 116 51253
R 2848	10K	1	MR25	4822 116 51253
R 2849	10K	1	MR25	4822 116 51253
R 2850	348	1	MR25	5322 116 54515
R 2851	511	1	MR25	4822 116 51282
R 2852	590	1	MR25	5322 116 50561
R 2853	4,42K	1	MR25	5322 116 50556
R 2854	1,87K	1	MR25	5322 116 50728
R 2855	51,1	1	MR25	5322 116 54442
R 2856	10K	1	MR25	4822 116 51253
R 2857	470	20	0,5W	5322 101 14047
R 2858	4,64K	1	MR25	5322 116 50484
R 2859	1K	20	0,5W	5322 100 10112
R 286	2,26K	1	MR25	5322 116 50675
R 2860	348	1	MR25	5322 116 54515
R 2861	1K	20	0,5W	5322 100 10112
R 2862	8,25K	1	MR25	5322 116 54558
R 2863	40,2	1	MR25	5322 116 50926
R 2864	1K	1	MR25	5322 116 54549
R 2866	40,2	1	MR25	5322 116 50926
R 2867	10K	20	0,5W	5322 100 10113
R 287	2,26K	1	MR25	5322 116 50675

POSNR	DESCRIPTION			ORDERING CODE
R 2901	1	1	MR25	4822 116 51179
R 2902	1	1	MR25	4822 116 51179
R 2903	22,6	1	MR25	5322 116 50491
R 2904	2,15	1	MR25	5322 116 55536
R 2907	5,11	1	MR25	5322 116 54192
R 2908	5,11	1	MR25	5322 116 54192
R 2909	1M	1	MR25	5322 116 55535
R 291	6,81K	1	MR25	4822 116 51252
R 2910	2,2K	20	0.5W	5322 101 14008
R 2911	100K	20	0.5W	5322 101 14071
R 2912	22,6K	1	MR25	5322 116 50481
R 2913	6,49K	1	MR25	5322 116 54603
R 2914	105K	1	MR25	5322 116 54698
R 2916	10K	1	MR25	4822 116 51253
R 2917	121K	1	MR25	5322 116 54704
R 2918	681	1	MR25	4822 116 51233
R 2919	2,49K	1	MR25	5322 116 50581
R 292	2,26K	1	MR25	5322 116 50675
R 2921	5,11K	1	MR25	5322 116 54595
R 2922	5,11K	1	MR25	5322 116 54595
R 2923	10K	1	MR25	4822 116 51253
R 2924	6,81K	1	MR25	4822 116 51252
R 2925	205	1	MR25	5322 116 50669
R 2926	1K	1	MR25	5322 116 54549
R 2927	1K	1	MR25	5322 116 54549
R 2928	1K	1	MR25	5322 116 54549
R 2929	1K	1	MR25	5322 116 54549
R 293	2,26K	1	MR25	5322 116 50675
R 2930	205	1	MR25	5322 116 50669
R 2931	1,21K	1	MR25	5322 116 54557
R 2932	27,4K	1	MR25	5322 116 50559
R 2933	2,05K	1	MR25	5322 116 50664
R 2934	511	1	MR25	4822 116 51282
R 2935	215	1	MR25	5322 116 55274
R 2936	205	1	MR25	5322 116 50669
R 2937	10	1	MR25	5322 116 50452
R 2938	2,05K	1	MR25	5322 116 50664
R 2939	30,1	1	MR25	5322 116 50904
R 294	82,5K	1	MR25	5322 116 54689
R 2940	100	1	MR25	5322 116 54469
R 2941	825	1	MR25	5322 116 54541
R 2942	2,15K	1	MR25	5322 116 50767
R 2943	511	1	MR25	4822 116 51282
R 2944	5,11K	1	MR25	5322 116 54595
R 2945	10	1	MR25	5322 116 50452
R 2946	5,11K	1	MR25	5322 116 54595
R 2947	4,64K	1	MR25	5322 116 50484
R 2948	205	1	MR25	5322 116 50669
R 2949	1,21K	1	MR25	5322 116 54557
R 2950	16,2	1	MR25	5322 116 54431
R 2951	205	1	MR25	5322 116 50669
R 2952	100	1	MR25	5322 116 54469
R 2953	3,01K	1	MR25	4822 116 51246
R 2954	10K	1	MR25	4822 116 51253
R 2955	249	1	MR25	5322 116 54499
R 2956	30,1K	1	MR25	5322 116 54655
R 2957	100	1	MR25	5322 116 54469
R 2958	10K	20	0,5W	5322 100 10113
R 2959	1K	1	MR25	5322 116 54549
R 296	82,5K	1	MR25	5322 116 54689
R 2960	681	1	MR25	4822 116 51233
R 2961	1K	1	MR25	5322 116 54549
R 2962	205	1	MR25	5322 116 50669
R 2963	205	1	MR25	5322 116 50669
R 2964	1K	1	MR25	5322 116 54549

POSNR	DESCRIPTION			ORDERING CODE
R 2965	287	1	MR25	5322 116 54506
R 2966	1K	1	MR25	5322 116 54549
R 2967	2,15K	1	MR25	5322 116 50767
R 2968	511	1	MR25	4822 116 51282
R 2969	1K	1	MR25	5322 116 54549
R 3	10K	20	0.1W	5322 101 24184
R 3001	249	1	MR25	5322 116 54499
R 3002	590	1	MR25	5322 116 50561
R 3003	33,2	1	MR25	5322 116 50527
R 3004	100	1	MR25	5322 116 54469
R 3005	40,2	1	MR25	5322 116 50926
R 3006	100	1	MR25	5322 116 54469
R 3007	24,9	1	MR25	5322 116 50903
R 3008	750	1	MR25	4822 116 51234
R 3009	2,2K	20	0.5W	5322 101 14008
R 3011	261	1	MR25	5322 116 54502
R 3012	274	1	MR25	5322 116 54504
R 3013	2,87K	1	MR25	5322 116 50414
R 3014	2,87K	1	MR25	5322 116 50414
R 3016	2,26K	1	MR25	5322 116 50675
R 3017	249	1	MR25	5322 116 54499
R 3018	3,83K	1	MR25	5322 116 54589
R 3019	75	1	MR25	5322 116 54459
R 3020	90,9	1	MR25	5322 116 54466
R 3021	178	1	MR25	5322 116 54492
R 3022	178	1	MR25	5322 116 54492
R 3023	100K	1	MR25	4822 116 51268
R 3024	6,81K	1	MR25	4822 116 51252
R 3026	11K	1	MR25	5322 116 54623
R 3027	75	1	MR25	5322 116 54459
R 3028	2,26K	1	MR25	5322 116 50675
R 3029	2,2K	20	0.5W	5322 101 14008
R 3030	3,32K	1	MR25	5322 116 54005
R 3031	90,9	1	MR25	5322 116 54466
R 3032	30,1	1	MR25	5322 116 50904
R 3033	30,1	1	MR25	5322 116 50904
R 3034	33,2	1	MR25	5322 116 50527
R 3036	619	1	MR25	5322 116 54529
R 3037	75	1	MR25	5322 116 54459
R 3038	215	1	MR25	5322 116 55274
R 3039	10K	20	0,5W	5322 100 10113
R 3040	36,5	1	MR25	5322 116 50409
R 3041	100	1	MR25	5322 116 54469
R 3043	1,96K	1	MR25	5322 116 54571
R 3044	100	1	MR25	5322 116 54469
R 3045	36,5	1	MR25	5322 116 50409
R 3046	619	1	MR25	5322 116 54529
R 3047	33,2	1	MR25	5322 116 50527
R 3048	187	1	MR25	5322 116 54494
R 3049	187	1	MR25	5322 116 54494
R 3050	127	1	MR16	5322 116 55396
R 3051	196	1	MR25	5322 116 55273
R 3052	10K	1	MR25	4822 116 51253
R 3053	402	1	MR25	5322 116 54519
R 3054	4,22K	1	MR25	5322 116 50729
R 3055	127	1	MR16	5322 116 55396
R 3056	220	20	0,5W	5322 101 14009
R 3057	1K	20	0,5W	5322 100 10112
R 3058	100	1	MR25	5322 116 54469
R 3059	2,15K	1	MR25	5322 116 50767
R 3061	1,78K	1	MR25	5322 116 50515
R 3063	2,87K	1	MR25	5322 116 50414
R 3064	2,87K	1	MR25	5322 116 50414
R 3066	33,2	1	MR25	5322 116 50527
R 3067	2,87K	1	MR25	5322 116 50414

POSNR	DESCRIPTION			ORDERING CODE
R 3068	75	1	MR25	5322 116 54459
R 3069	2,87K	1	MR25	5322 116 50414
R 3071	12,7K	1	MR25	5322 116 50443
R 3072	7,5K	1	MR25	5322 116 54608

POSNR	DESCRIPTION	ORDERING CODE
V 401	BAW62	4822 130 30613
V 402	BAW62	4822 130 30613
V 601	BAW62	4822 130 30613
V 602	BAW62	4822 130 30613
V 701	BAW62	4822 130 30613
V 901	BAW62	4822 130 30613
V 1	D14-292GH/39	5322 131 24086
V 1001	BC558B	4822 130 44197
V 1002	BC558B	4822 130 44197
V 1003	BC558B	4822 130 44197
V 1004	BC549C	4822 130 44246
V 1006	BC549C	4822 130 44246
V 1007	BC549C	4822 130 44246
V 1008	BAW62	4822 130 30613
V 1009	BAW62	4822 130 30613
V 1011	BAW62	4822 130 30613
V 1012	BSX20	5322 130 40417
V 1013	BZV13	5322 130 34301
V 1014	BZX79-C5V6	4822 130 34173
V 1016	BZX79-C5V6	4822 130 34173
V 1017	BSX20	5322 130 40417
V 1018	BD435	4822 130 40982
V 1019	BD436	4822 130 40995
V 1021	BC549C	4822 130 44246
V 1101	BF324	4822 130 41448
V 1102	BAW62	4822 130 30613
V 1103	BZV13	5322 130 34301
V 1104	BF199	4822 130 44154
V 1106	BC549C	4822 130 44246
V 1108	BF324	4822 130 41448
V 1109	BZY88-C3V3	5322 130 30392
V 1111	BC549C	4822 130 44246
V 1112	BAW62	4822 130 30613
V 1113	BF324	4822 130 41448
V 1114	BF199	4822 130 44154
V 1116	BZX79-C6V2	4822 130 31111
V 1117	BF324	4822 130 41448
V 1201	BAW62	4822 130 30613
V 1301	BAW62	4822 130 30613
V 1302	BZX79-C30	4822 130 34328
V 1303	BC558	4822 130 40941
V 1304	BD435	4822 130 40982
V 1501	BD237	4822 130 44235
V 1502	BY409A	5322 130 34594
V 1503	BYX55-600	4822 130 30817
V 1504	BYX55-600	4822 130 30817
V 1506	BYX55-600	4822 130 30817
V 1507	BYX55-600	4822 130 30817
V 1508	BYX55-600	4822 130 30817
V 1509	BYX55-600	4822 130 30817
V 1511	BYW29-150	5322 130 34711
V 1512	BYW29-150	5322 130 34711
V 1513	BAX12A	5322 130 34605
V 1514	BAX12A	5322 130 34605
V 1516	BAX12A	5322 130 34605
V 1517	BAX12A	5322 130 34605

POSNR	DESCRIPTION	ORDERING CODE
V 1518	BYW29-150	5322 130 34711
V 1519	BYW29-150	5322 130 34711
V 1521	BY208-800	4822 130 31348
V 1522	BY208-800	4822 130 31348
V 1523	BC549C	4822 130 44246
V 1524	BSS38	4822 130 40968
V 1526	BSS38	4822 130 40968
V 1527	BRY39	5322 130 40482
V 1528	BY208-800	4822 130 31348
V 1529	BY208-800	4822 130 31348
V 1531	BC549C	4822 130 44246
V 1532	BSS68	5322 130 44247
V 1533	BSS68	5322 130 44247
V 1534	BZX79-C4V7	4822 130 34174
V 1536	BSS38	4822 130 40968
V 1537	BSS38	4822 130 40968
V 1538	BC559B	4822 130 44358
V 1539	BC549C	4822 130 44246
V 1541	BC549C	4822 130 44246
V 1542	BZX75-C1V4	4822 130 34047
V 1543	BAW62	4822 130 30613
V 1544	1N823	5322 130 34405
V 1546	BAW62	4822 130 30613
V 1547	BC549C	4822 130 44246
V 1548	BYW29-150	5322 130 34711
V 1549	BD237	4822 130 44235
V 1551	BT151-500R	5322 130 24081
V 1552	BAW62	4822 130 30613
V 1553	BC549C	4822 130 44246
V 1554	BZX79-C47	4822 130 34383
V 1556	BZX79-C47	4822 130 34383
V 1557	BYW29-150	5322 130 34711
V 1558	BC559B	4822 130 44358
V 1559	BC549C	4822 130 44246
V 1561	BD237	4822 130 44235
V 1562	BYW29-150	5322 130 34711
V 1563	BYW29-150	5322 130 34711
V 1564	BC549C	4822 130 44246
V 1601	BY208-1000	4822 130 31051
V 1602	BY224-600	5322 130 34761
V 1603	BAX12A	5322 130 34605
V 1604	BAX12A	5322 130 34605
V 1606	BAX12A	5322 130 34605
V 1607	BAX12A	5322 130 34605
V 1608	BY208-1000	4822 130 31051
V 1609	BY208-1000	4822 130 31051
V 1611	BZX79-C12	4822 130 34197
V 1612	BZX79-C12	4822 130 34197
V 1613	BZX79-C12	4822 130 34197
V 1614	BAW62	4822 130 30613
V 1616	BC547B	4822 130 40959
V 1617	BAX12A	5322 130 34605
V 1618	BU208A	4822 130 31171
V 1619	BAW62	4822 130 30613
V 1621	BUX86	5322 130 44718
V 1622	BC549C	4822 130 44246
V 2001	BC547B	4822 130 40959
V 2002	FH1100	5322 130 34062
V 2003	FH1100	5322 130 34062
V 2004	BAW62	4822 130 30613
V 2006	BC556	4822 130 40989
V 2007	BF423	4822 130 41646
V 2008	FH1100	5322 130 34062
V 2009	FH1100	5322 130 34062
V 2011	BAW62	4822 130 30613

POSNR	DESCRIPTION	ORDERING CODE
V 2012	BAW62	4822 130 30613
V 2013	BC556	4822 130 40989
V 2014	BAV21	4822 130 30842
V 2016	BF422	4822 130 44108
V 2017	BZX79-B6V2	4822 130 34167
V 2018	BZX79-C10	4822 130 34297
V 2019	BAW62	4822 130 30613
V 2021	BC547B	4822 130 40959
V 2022	BZX79-B6V2	4822 130 34167
V 2023	BF422	4822 130 44108
V 2024	BAW62	4822 130 30613
V 2026	BZX79-C10	4822 130 34297
V 2027	BAW62	4822 130 30613
V 2028	BC549C	4822 130 44246
V 2029	BZX79-B6V8	4822 130 34278
V 2031	BAV21	4822 130 30842
V 2032	BF423	4822 130 41646
V 2033	BC549C	4822 130 44246
V 2034	BC549C	4822 130 44246
V 2036	BZX79-C6V8	4822 130 34278
V 2037	BZX79-C6V8	4822 130 34278
V 2038	BC549C	4822 130 44246
V 2039	BZX79-C6V8	4822 130 34278
V 2041	BZX79-C6V8	4822 130 34278
V 2042	BZX79-C6V8	4822 130 34278
V 2043	BZX79-C6V8	4822 130 34278
V 2400	BAW62	4822 130 30613
V 2401	BSV80	5322 130 34044
V 2402	BAW62	4822 130 30613
V 2403	BAW62	4822 130 30613
V 2404	BAW62	4822 130 30613
V 2405	BAW62	4822 130 30613
V 2406	BFW30	5322 130 40379
V 2407	BC264A	5322 130 44476
V 2408	BC549C	4822 130 44246
V 2409	BAW62	4822 130 30613
V 241	BZX79-C5V1	4822 130 34233
V 2410	BAW62	4822 130 30613
V 2411	BAW62	4822 130 30613
V 2412	BAV45	5322 130 34037
V 2413	BC549C	4822 130 44246
V 2414	BC559B	4822 130 44358
V 2415	BC549C	4822 130 44246
V 2416	BC559B	4822 130 44358
V 2417	BC559B	4822 130 44358
V 2418	BF324	4822 130 41448
V 2419	BF324	4822 130 41448
V 242	BZX79-C5V1	4822 130 34233
V 2420	BC549C	4822 130 44246
V 2421	BAW62	4822 130 30613
V 2422	BC549C	4822 130 44246
V 2423	BAW62	4822 130 30613
V 2424	BF324	4822 130 41448
V 2426	BF324	4822 130 41448
V 2427	BAW62	4822 130 30613
V 2428	BC559B	4822 130 44358
V 2429	BC549C	4822 130 44246
V 2432	BC549C	4822 130 44246
V 2433	BC559B	4822 130 44358
V 2434	BZX75-C1V4	4822 130 34047
V 2436	BC549C	4822 130 44246
V 2437	BAW62	4822 130 30613
V 2438	BC549C	4822 130 44246
V 2439	BC549C	4822 130 44246
V 2441	BC549C	4822 130 44246

POSNR	DESCRIPTION	ORDERING CODE
V 2442	BC549C	4822 130 44246
V 2443	BC549C	4822 130 44246
V 2444	BC559B	4822 130 44358
V 2446	BAW62	4822 130 30613
V 2448	BFW30	5322 130 40379
V 2449	BC559B	4822 130 44358
V 2450	BC549C	4822 130 44246
V 2451	BC264A	5322 130 44476
V 2452	BAW62	4822 130 30613
V 2453	BAW62	4822 130 30613
V 2454	BAV45	5322 130 34037
V 2456	BC559B	4822 130 44358
V 2457	BC559B	4822 130 44358
V 2458	BAW62	4822 130 30613
V 2459	BC559B	4822 130 44358
V 2461	BAW62	4822 130 30613
V 2462	BF324	4822 130 41448
V 2463	BAW62	4822 130 30613
V 2464	BC549C	4822 130 44246
V 2466	BF324	4822 130 41448
V 2467	BAW62	4822 130 30613
V 2468	BC559B	4822 130 44358
V 2469	BC549C	4822 130 44246
V 2471	BC549C	4822 130 44246
V 2473	BC549C	4822 130 44246
V 2474	BC559B	4822 130 44358
V 2476	BC549C	4822 130 44246
V 2477	BAW62	4822 130 30613
V 2478	BZX75-C2V1	4822 130 34049
V 2479	BZX75-C2V8	4822 130 34048
V 2480	BZX79-C9V1	4822 130 30862
V 2481	BAW62	4822 130 30613
V 2483	BAW62	4822 130 30613
V 2484	BAW62	4822 130 30613
V 2485	BZX75-C1V4	4822 130 34047
V 2486	BAW62	4822 130 30613
V 2487	BAW62	4822 130 30613
V 2701	BC264A	5322 130 44476
V 2702	BFY90	4822 130 40493
V 2703	BC559B	4822 130 44358
V 2704	BAW62	4822 130 30613
V 2706	BAW62	4822 130 30613
V 2707	BF324	4822 130 41448
V 2708	BC549C	4822 130 44246
V 2709	BAW62	4822 130 30613
V 2711	BF324	4822 130 41448
V 2712	BC549C	4822 130 44246
V 2713	BAW62	4822 130 30613
V 2714	BAW62	4822 130 30613
V 2716	BAW62	4822 130 30613
V 2717	BC549C	4822 130 44246
V 2718	BC549C	4822 130 44246
V 2719	BAW62	4822 130 30613
V 2721	BAW62	4822 130 30613
V 2722	BAW62	4822 130 30613
V 2723	BC559B	4822 130 44358
V 2724	BC549C	4822 130 44246
V 2726	BF199	4822 130 44154
V 2727	BC549C	4822 130 44246
V 2728	BC559B	4822 130 44358
V 2729	BC549C	4822 130 44246
V 2731	BF199	4822 130 44154
V 2732	BC549C	4822 130 44246
V 2733	BF450	4822 130 44237
V 2734	BAW62	4822 130 30613

POSNR	DESCRIPTION	ORDERING CODE
V 2736	BC549C	4822 130 44246
V 2737	BC549C	4822 130 44246
V 2738	BAW62	4822 130 30613
V 2739	BAW62	4822 130 30613
V 2741	BC549C	4822 130 44246
V 2742	BC549C	4822 130 44246
V 2743	BAW62	4822 130 30613
V 2744	BAW62	4822 130 30613
V 2746	BC549C	4822 130 44246
V 2747	BC549C	4822 130 44246
V 2748	BAW62	4822 130 30613
V 2749	BF450	4822 130 44237
V 2751	BC549C	4822 130 44246
V 2752	BZX75-C2V1	4822 130 34049
V 2753	BC559B	4822 130 44358
V 2754	BC559B	4822 130 44358
V 2756	BF324	4822 130 41448
V 2757	BF324	4822 130 41448
V 2758	BF324	4822 130 41448
V 2759	BF324	4822 130 41448
V 2761	BF450	4822 130 44237
V 2762	BC549C	4822 130 44246
V 2763	BC549C	4822 130 44246
V 2764	BC559B	4822 130 44358
V 2901	BAW62	4822 130 30613
V 2902	BAW62	4822 130 30613
V 2903	BZV10	5322 130 34439
V 2904	BAW62	4822 130 30613
V 2905	BZX75-C1V4	4822 130 34047
V 2906	BAW62	4822 130 30613
V 2907	BAW62	4822 130 30613
V 2908	BC559B	4822 130 44358
V 2909	BAW62	4822 130 30613
V 2911	BAW62	4822 130 30613
V 2912	BAW62	4822 130 30613
V 2913	BSX20	5322 130 40417
V 2914	BAW62	4822 130 30613
V 2915	BZX75-C1V4	4822 130 34047
V 2916	BSX20	5322 130 40417
V 2917	BC559B	4822 130 44358
V 2918	BC559B	4822 130 44358
V 2919	BAW62	4822 130 30613
V 2920	BAW62	4822 130 30613
V 2921	BZV10	5322 130 34439
V 2922	BC559B	4822 130 44358
V 3001	BFQ24	5322 130 41664
V 3002	BFQ24	5322 130 41664
V 3003	BC549C	4822 130 44246
V 3004	BC549C	4822 130 44246
V 3006	BC559B	4822 130 44358
V 3007	BC559B	4822 130 44358
V 3008	BC559B	4822 130 44358
V 3009	BC549C	4822 130 44246
V 3010	BZX79-C5V6	4822 130 34173
V 3011	BZV13	5322 130 34301
V 3012	BZV13	5322 130 34301

1.2.2.7. Miscellaneous

Item	Ordering number	Type/Description
B1	5322 130 34875	Led red cqy 54 – 111
B2	5322 130 34875	Led red cqy 54 – 111
B3	5322 130 34875	Led red cqy 54 – 111
B4	5322 130 34875	Led red cqy 54 – 111
B5	5322 130 34875	Led red cqy 54 – 111
B6	5322 130 34875	Led red cqy 54 – 111
B7	5322 130 34875	Led red cqy 54 – 111
B8	5322 130 34875	Led red cqy 54 – 111
B9	5322 130 34875	Led red cqy 54 – 111
B10	5322 130 34971	DL1414D Display
B11	5322 130 34971	DL1414D Display
B12	5322 130 34971	DL1414D Display
B13	4822 134 40167	Lamp 5 V 60 mA
B14	4822 134 40167	Lamp 5 V 60 mA
B15	5322 130 34875	Led red cqy 54 –111
B16	5322 130 34875	Led red cqy 54 – 111
B17	4822 134 40167	Lamp 5 V 60 mA
B18	4822 134 40167	Lamp 5 V 60 mA
B19	4822 134 40167	Lamp 5 V 60 mA
B20	4822 134 40167	Lamp 5 V 60 mA
B21	5322 130 34971	DL1414D Display
B22	5322 130 34875	Led red cqy 54 – 111
B23	5322 130 34875	Led red cqy 54 – 111
B24	4822 130 31144	Led red cqy 24B
B401	5322 242 74397	CRYSTAL 5MC
E1	5322 134 44177	Lamp 28 V - 80 mA
E2	5322 134 44177	Lamp 28 V - 80 mA
F1701	4822 253 30025	Fuse
K2401...K2418	5322 280 24126	Reed contact
K2401...K2418	5322 156 14076	Reed coil
K2701	5322 280 24131	Reed relay assy
L1101	5322 158 10283	Microchoke 150 μH
L1102	5322 156 14101	Coil
L1103	5322 156 14101	Coil
L1104	5322 156 14101	Coil
L1106	5322 156 14101	Coil
L1501 L1502 L1503 L1504	4822 152 20486	Choke AT 4043-15
L1506	5322 152 24095	Choke TFU-15
L1508 L1509	5322 152 24094	Choke TFU-15
L1601	5322 281 64154	Coil
L1602	5322 152 24062	Choke
L1603	5322 156 14076	Coil
L1604	5322 156 14076	Coil
L2401 L2402 L2403 L2404	5322 156 14076	Coil

Item	Ordering number	Type/Description
L2406 L2407 L2408 L2409 L2411 L2412	5322 158 14283	Coil assy.
S1	5322 276 44099	Pushbutton switch
S8	5322 276 34063	Pushbutton switch
S11	5322 276 34064	Pushbutton switch
S14	5322 276 74026	Pushbutton switch
S20	5322 278 64015	Rotary switch
S22	5322 278 64015	Rotary switch
S23	5322 278 64015	Rotary switch
S29	5322 276 44084	Pushbutton switch
S30	5322 276 74037	Pushbutton switch
S37	5322 276 44085	Pushbutton switch
S39	5322 276 44086	Pushbutton switch
S45	5322 277 24071	Mains voltage adaptor
S201	5322 263 64007	Plug (jumper)
S1201	5322 263 64007	Plug (jumper)
S1801	4822 277 10348	Switch assy.
T1501	5322 142 64104	Transformer
T1601	5322 148 80048	Transformer
T1602	5322 146 34126	Transformer
T1603	5322 142 44026	Transformer
V1	5322 131 24086	C.R.T. D14-292GH/39
X1	5322 267 14014	CAL socket
X2	5322 405 94073	CAL current loop
X3	5322 267 10004	HF-CON BNC Female
X4	5322 267 14037	Connector
X5	5322 535 84446	Threaded end
X6	5322 267 10004	HF-CON BNC Female
X7	5322 268 14157	Contact
X8	5322 268 14157	Contact
X259	5322 267 74111	Plug female
X1606	4822 266 30071	Plug
Z1701	5322 121 44261	Mains filter

1.2.2.8. Connectors

Ordering number	Description
5322 265 64082	64-pole connector male (PLUG-IN UNITS)
5322 267 74092	64-pole connector female (PLUG-IN UNITS)
5322 267 64007	CIS connectors male
5322 267 64031	CIS connectors bottom entry
5322 265 54006	CIS connectors top entry
5322 290 34123	Soldering pin for measuring points
4822 267 50268	CIS connector male
5322 268 24116	Coaxial socket, vertically mounted on pc boards
4822 265 30121	3-pole socket (stocko MKS 823-1-0-303)
5322 268 24133	Delay line connectors

1.2.2.9. IEC 625-1 bus interface unit A14 (PM3325).

Item	Ordering number	Description			
		CAPACITORS			
C 1401	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1402	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1403	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1404	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1406	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1407	4822 122 31173	CAPACITOR,CERAM	220PF	10%	500V
C 1408	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1409	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1411	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1412	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1413	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1414	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1416	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1417	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1418	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1419	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1421	4822 122 31054	CAPACITOR,CERAM	10PF	2%	100V
C 1422	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1423	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1424	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1426	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1427	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1428	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1429	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1431	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1432	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1433	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1434	4822 122 31414	CAPACITOR,CERAM	10NF		100V
C 1436	4822 122 31173	CAPACITOR,CERAM	220PF	10%	500V
C 1437	4822 124 20699	CAP,ELECTROLYT	47UF	50%	25V
		RESISTORS			
R 1401	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1402	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1403	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W
R 1404	5322 116 50608	RESISTOR,M.FILM	6K19	1%	0,4W

Item	Ordering number	Description
	INTEGRATED CIRCUITS	
D 1401	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1402	5322 209 84996	INTEGR.CIRCUIT SN74LS10N
D 1403	5322 209 85311	INTEGR.CIRCUIT N74LS32A
D 1404	5322 209 84995	INTEGR.CIRCUIT SN74LS08N
D 1406	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1407	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1408	5322 209 14509	INTEGR.CIRCUIT HEF4738VP
D 1409	5322 209 85266	INTEGR.CIRCUIT SN74LS123N
D 1411	5322 209 85312	INTEGR.CIRCUIT N74LS02A
D 1412	5322 209 85266	INTEGR.CIRCUIT SN74LS123N
D 1413	5322 209 85562	INTEGR.CIRCUIT
D 1414	5322 209 85752	INTEGR.CIRCUIT N74LS155N
D 1416	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1417	5322 209 85464	INTEGR.CIRCUIT MC3441P
D 1418	5322 209 84997	INTEGR.CIRCUIT SN74LS86N
D 1419	5322 209 85346	INTEGR.CIRCUIT SN74LS279N
D 1421	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1422	5322 209 84823	INTEGR.CIRCUIT N74LS00N
D 1423	5322 209 86017	INTEGR.CIRCUIT SN74LS244N
D 1424	5322 209 86062	INTEGR.CIRCUIT
D 1426	5322 209 86062	INTEGR.CIRCUIT
D 1427	5322 209 86062	INTEGR.CIRCUIT
D 1428	5322 209 86017	INTEGR.CIRCUIT SN74LS244N
D 1429	5322 209 14219	INTEGR.CIRCUIT HEF4014BP
D 1431	5322 209 14219	INTEGR.CIRCUIT HEF4014BP
		MISCELLANEOUS
S 1401	5322 277 24045	SWITCH
S 1402	5322 277 24045	SWITCH
S 1403	5322 277 24045	SWITCH
S 1404	5322 277 24045	SWITCH
S 1405	5322 277 24045	SWITCH
S 1406	5322 277 24045	SWITCH
S 1407	5322 277 24053	SWITCH,SLIDE
X 1401	5322 265 64082	SOCKET,MALE
A80	5322 321 20474	CABLE,CONNECT.
D407	5322 209 10151	INTEGR.CIRCUIT
	5322 500 10265	NUT

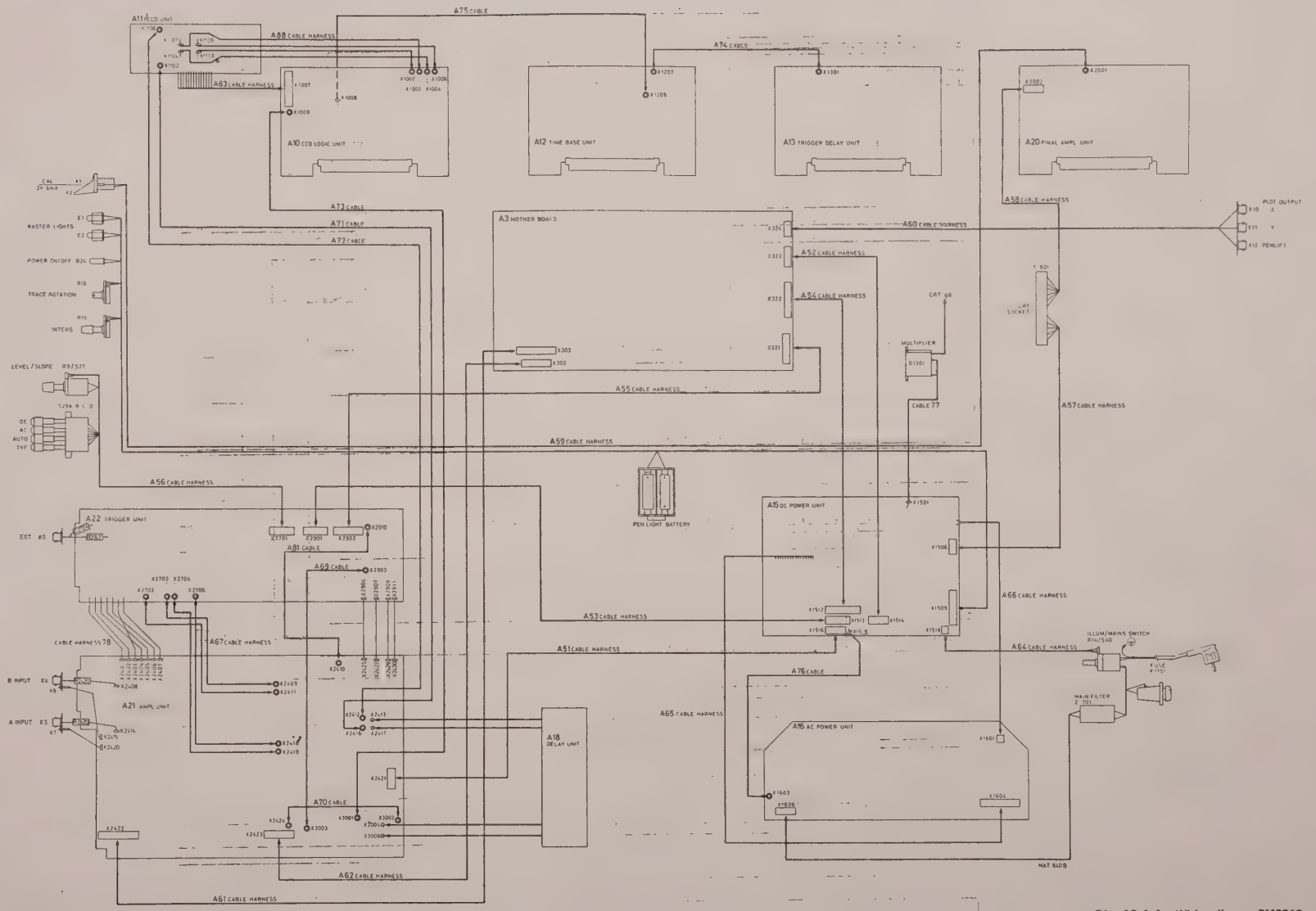

Fig. 13.1.1. Wiring diagram PM3310

ASSESSMENT OF T & M INSTRUMENTS

(excl. potentiometric recorders)

The information contents of the coded failure description is necessary for our computerized processing of quality data.

Since the reporting of repair and maintenance routines must be complete and exact, we give you an example of a correctly filled-out PHILIPS SERVICE Job sheet.

① Country	② Day Month Year	③ Typenumber /Version	④ Factory/Serial no.
3 2	1 5 0 4 7 5	0 P M 3 2 6 0 0 2	D O 0 0 7 8 3

CODED FAILURE DESCRIPTION ⑥

⑤ Nature of call	Location	Component/sequence no.	Category
☐ Installation		T S 0 6 0 7	5
☐ Pre sale repair		R 0 0 6 3 1	2
☐ Preventive maintenance	0 0 2 1	9 9 0 0 0 1	4
☒ Corrective maintenance			
☐ Other			

⑦ *Job completed* ☒

Working time ⑧ ☐☐12 Hrs

Detailed description of the information to be entered in the various boxes:

①Country: 3 2 = Switzerland

②Day Month Year 1 5 0 4 7 5 = 15 April 1975

③Type number/Version O P M 3 2 6 0 0 2 = Oscilloscope PM 3260, version 02 (in later oscilloscopes this number is placed in front of the serial no)

④Factory/Serial number D O 0 0 7 8 3 = DO 783 These data are mentioned on the type plate of the instrument

⑤ Nature of call: Enter a cross in the relevant box

⑥ Coded failure description

Location

☐☐☐☐

These four boxes are used to isolate the problem area. Write the code of the part in which the fault occurs, e.g. unit no or mechanical item no of this part (refer to 'PARTS LISTS' in the manual).

Example: 0001 for Unit 1
000A for Unit A
0075 for item 75

If units are not numbered, do not fill in the four boxes; see Example Job sheet.

Component/sequence no.

☐☐☐☐☐☐

These six boxes are intended to pinpoint the faulty component.

A. Enter the component designation as used in the circuit diagram. If the designation is alfa-numeric,the letters must be written (starting from the left) in the two left-hand boxes and the figures must be written (in such a way that the last digit occupies the right-most box) in the four right-hand boxes.

B. Parts not identified in the circuit diagram:

990000 Unknown/Not applicable
990001 Cabinet or rack (text plate, emblem, grip, rail, graticule, etc.)
990002 Knob (incl. dial knob, cap, etc.)
990003 Probe (only if attached to instrument)
990004 Leads and associated plugs
990005 Holder (valve,transistor, fuse, board, etc.)
990006 Complete unit (p.w. board, h.t. unit, etc.)
990007 Accessory (only those without type number)
990008 Documentation (manual, supplement, etc.)
990009 Foreign object
990099 Miscellaneous

Category

☐

0 Unknown, not applicable (fault not present, intermittent or disappeared)
1 Software error
2 Readjustment
3 Electrical repair (wiring, solder joint, etc.)
4 Mechanical repair (polishing, filing, remachining, etc.)
5 Replacement (of transistor, resistor, etc.)
6 Cleaning and/or lubrication
7 Operator error
8 Missing items (on pre-sale test)
9 Environmental requirements are not met

⑦ Job completed: Enter a cross when the job has been completed.

⑧ Working time: Enter the total number of working hours spent in connection with the job (excluding travelling, waiting time, etc.), using the last box for tenths of hours.

☐☐12 = 1,2 working hours (1 h 12 min.)